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THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER SEPTEMBER 1977 • VOLUME 16 • NUMBER 9

FEATURES

83 COMPARISONS AND TRENDS IN MICROPROCESSOR ARCHITECTURE by Edwin E. Klingman

By classifying available microprocessor architectures into just two categories, an overview of the entire microprocessor spectrum is evolved for relative performance analysis and future direction

95 AN UPDATE ON MOS ROMs

by David Huffman

Current ROM technology is investigated in an attempt to point out how manufacturers have overcome problems such as slow access time, high power dissipation, and long prototype and production cycles

105 MICROPROCESSOR SYSTEM VALIDATION AND FAILURE ISOLATION WITH PORTABLE TESTER

by John W. Neese

On-site microprocessor fault detection or performance verification is realized using a handheld keyboard and a programmable PC board. Designed to check out a specific microprocessor, the unit presents a cost-effective solution to testing problems

114 AN INTERACTIVE SOFTWARE PROGRAM FOR A STANDALONE GRAPHIC SYSTEM

by Robert I. Ross

Both 2-port circuit analysis and circuit design can be performed under manual or automatic control by resident software in an integral graphic display system for polar, rectangular, or Smith grid presentations

120a DESIGNER'S GUIDE FOR SELECTING MAGNETIC MINI-MEDIA

by A. Bruce Manildi

Determining which magnetic mini-medium is best suited for recording data in a particular application is simplified for designers by assessing performance characteristics and relative costs

168 COMMUNICATIONS PROCESSOR FULFILLS MULTIPLICITY OF DUTIES UNDER PROGRAM CONTROL

Microprocessor controller and optional function boards enable turnkey data communications processor to perform as universal device, with specific duties dictated by resident software

DEPARTMENTS

- 6 CALENDAR
- 12 LETTERS TO THE EDITOR
- 18 COMMUNICATION CHANNEL
- 34 DIGITAL TECHNOLOGY REVIEW
- 54 DIGITAL CONTROL AND AUTOMATION SYSTEMS
- 124 MICRO PROCESSOR/ COMPUTER DATA STACK
- 148 AROUND THE IC LOOP
- 172 PRODUCTS
- 194 LITERATURE
- 195 GUIDE TO PRODUCT INFORMATION
- 198 ADVERTISERS' INDEX

Reader Service Cards pages 201-204



8

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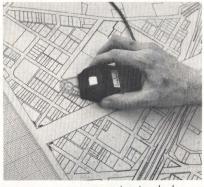
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- OCT 4, OCT 27, and NOV 17—Invitational Computer Conf, Radisson Hotel, Minneapolis, Minn; Cabana Hyatt House, Palo Alto, Calif; Houston Oaks, Houston, Tex. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037
- OCT 4-6—NEPCON Central '77 (Nat'l Electronics Packaging and Production Conf), O'Hare Internat'| Trade and Exposition Ctr, and Hyatt Regency O'Hare Hotel, Rosemont, III. INFORMATION: Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866
- OCT 9-15—INTELCOM '77 (Internat'I Telecommunications Exposition), Atlanta, Ga. INFORMATION: Barbara Coffin, Promotion Mgr, Horizon House Internat'I, 610 Washington St, Dedham, MA 02026. Tel: 1-800-225-9977, (617) 326-8220
- OCT 10-13—10th Conv of Electrical and Electronic Engineers in Israel, Tel Aviv. INFORMATION: Daphna Knassim Ltd, 444 Madison Ave, New York, NY 10022. Tel: (212) 688-7072
- OCT 10-14—IEEE Internat'l Sym on Information Theory, ILR Conf Ctr, Cornell U, Ithaca, NY. INFORMATION: Prof Toby Berger, Dept of Electrical Engineering, 208 Phillips Hall, Cornell U, Ithaca, NY 14853
- OCT 17-19—ACM 1977 Annual Conf (Assoc for Computing Machinery), Olympic Hotel, Seattle, Wash. INFORMATION: Dr James S. Ketchel, PO Box 16156, Seattle, WA 98116. Tel: (206) 935-6776, (206) 623-4987
- OCT 17-20—ISA/77 (Instrument Society of America Conf & Exhibit), Internat'l Conv Ctr, Niagara Falls, NY. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171
- OCT 18-19—NASA Marshall Space Flight Ctr/U of Alabama, Huntsville Data Management Sym, Marshall Flight Ctr, Huntsville, Ala. INFORMATION: Gen'I Chm, Data Mgmt Workshop, Johnson Environmental & Energy Ctr, U of Alabama, PO Box 1247, Huntsville, AL 35807. Tel: (205) 895-6361
- OCT 19-20—10th Annual Electrical Connector Sym, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014
- OCT 25-27—Semiconductor Test Sym, Cherry Hill, NJ. INFORMATION: Mrs R. J. Sunder-

- land, Secretary and Registrar, Test Symposium Committee, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 424-2400
- OCT 28—Society for Information Display (SID) One-Day Technical Conf, Sheraton Inn/Airport, San Diego, Calif. INFORMA-TION: Dan Heflinger, DatagraphiX, Inc, PO Box 82449, San Diego, CA 92138. Tel: (714) 291-9960
- OCT 31-NOV 2—AIAA/IEEE/NASA Computers in Aerospace, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Hugh Harrington, Dept E411, McDonnell Douglas Astronautics, PO Box 516, St Louis, MO 63166. Tel: (314) 232-9102
- OCT 31-NOV 2—18th Annual IEEE Sym on Foundations of Computer Science, Marriott Inn, Providence, RI. INFORMATION: Prof John E. Savage, FOCS '77, Program in Computer Science, Box D, Brown U, Providence, RI 02912. Tel: (401) 863-2601
- NOV 2-4—AUTOTESTCON '77 (IEEE Internat'l Automatic Testing Conf), Dunfey's Resort, Hyannis, Mass. INFORMATION: Eugene B. Galton, Gen'l Chm, AUTOTESTCON '77, RCA Corp, PO Box 588, Burlington, MA 01803. Tel: (617) 272-4000
- NOV 7-11—Electronic Components '77, U.S. Trade Ctr, London, England. INFORMATION: Robert Connan, Office of Internat'l Mktg, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3465
- NOV 8-10—Compec UK '77 (Computer Peripherals Exhibition), Wembley Centre, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1-9LU, England
- NOV 8-10—MIDCON, O'Hare Conv Ctr and Hyatt Regency Hotel, Chicago, III. INFOR-MATION: W. C. Weber, Jr, IEEE, 999 Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965
- NOV 8-10—Canadian Computer Show Conf, Internat'l Ctr of Commerce, Toronto, Canada. INFORMATION: Derek Tidd, Show Mgr, Industrial and Trade Shows of Canada, 481 University Ave, Toronto, Ontario M5W LA7, Canada
- NOV 8-11—23rd Annual Conf on Magnetism and Magnetic Materials, Radisson Hotel, Minneapolis, Minn. INFORMATION: C. D. Graham, Jr, Dept of Metallurgy and Materials, U of Penn, Philadelphia, PA 19174
- NOV 8-11—COMPSAC '77 (IEEE Computer Soc Software & Applications Conf), Sheraton-O'Hare Motor Hotel, Chicago, III. INFORMATION: Prof Stephen S. Yau, Dept of Computer Science, Northwestern U, Evanston, IL 60201. Tel: (312) 492-3641
- NOV 15-17—6th Annual Meeting of Members of Computer Aided Manufacturing-Internat'l, Inc (CAM-I), Americana Inn, Arlington, Tex. INFORMATION: C. H. Link, Exec Secretary and Gen'l Mgr, CAM-I, 611

- Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: (817) 265-5328
- DEC 5-7—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Susan Hinman, Courtesy Assoc, 1629 K St, NW, Washington, DC 20006. Tel: (202) 296-8100
- DEC 5-10—OFISISTEMA '77 (U.S. Exhibition of Advanced Business Equipment, Computers, and Peripherals), Caracas, Vénezuela. INFORMATION: Hans J. Amrhein, Project Mgr, Rm 4036, Office of Internat'l Mktg, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-2332, (202) 377-2995

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- OCT 3-6—Internat'l Purdue Workshop on Industrial Computer Systems, Purdue U, West Lafayette, Ind. INFORMATION: Prof T. J. Williams, Purdue Lab for Applied Industrial Control, 102 Michael Golden, Purdue U, West Lafayette, IN 47907. Tel: (317) 494-8425
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- SEPT 26-30—Small Computer Systems; OCT 3-7—Digital Signal Processing, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106, 1-800-424-9773
- OCT 15—14th Annual Patent Institute, Fairleigh Dickinson U, Madison, NJ. IN-FORMATION: Joseph L. Tramutola, Jr, Director, 1977 Patent Institute, Fairleigh Dickinson U, 285 Madison Ave, Madison, NJ 07940. Tel: (201) 377-4700, X423

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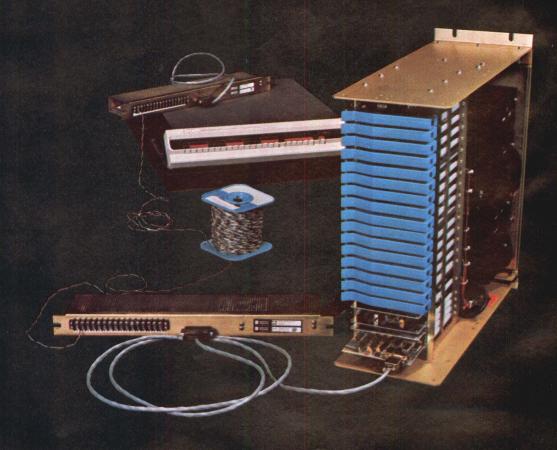
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The Microprocessor Lab also offers three emulation modes for system-controlled, partial, and full emulation . . . on the same microprocessor you'll be using in the finished product. A memory mapping technique for gradually releasing program functions to the prototype and systematically isolating program errors. A real-time trace option which allows you to monitor microprocessor activity at full speed.

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A Typical Development Sequence Using The 8001

The initial design cycle has been completed. Software and hardware functions have been assigned; prototype hardware has been built and preliminary debugging checks have been run using the 8001; software has been developed and partially debugged on an external software development system. The program is downloaded to the Microprocessor Lab through any RS-232-C compatible medium (such as modem or paper tape), and the critical integration phase begins.

The program is first tested in system-controlled emulation (mode 0) on the 8001 emulator processor. This "dry run" enables you to detect any software errors that may not have shown up at the assembly level.

In partial and full emulation (modes 1 and 2), the program is exercised on the prototype with the 8001 prototype control probe connected to the



emulator processor at one end and plugged into the empty micro-processor socket in prototype circuitry at the other. This lets you integrate in stages while you maintain control through the 8001.

In partial emulation, the program runs using 8001 memory space and prototype I/O and clock. With the memory mapping feature, memory may be mapped over to the prototype by address blocks. This enables you to localize program errors... or even "patch" around a faulty bit or routine. Throughout partial emulation, program activity may be accessed via the powerful 8001 debugging system, which allows you to trace, set breakpoints, examine and change memory and register contents.

In full emulation, the program is exercised on the now stand-alone prototytpe; you still maintain complete control through the Microprocessor Lab. All I/O and timing functions are directed by the prototype; all memory has been mapped over to the prototype; and only the prototype control probe is still in place, emulating the target microprocessor. Although the prototype is effectively freestanding, then, you still direct program activity, at the prototype end of the probe, from the 8001.

Real-Time Trace

With the optional real time prototype analyzer, you can dynamically monitor the prototype address bus, data bus, and up to eight other locations on the prototype circuit board. Prototype activity is monitored at full speed, without stopping or slowing up the working microprocessor. This enables you to locate critical timing problems and hardware/software sequence problems during partial and full emulation.

In this way, the 8001 provides a total hardware debugging environment supporting each successive phase of the product development cycle. After downloading object code, the designer proceeds from hardware test and software debugging, to the sequential integration of program and circuit, to final integration and test of the stand-alone product. The real-time prototype analyzer enhances partial and full emulation by allowing the user to monitor and access prototype activity in real time.

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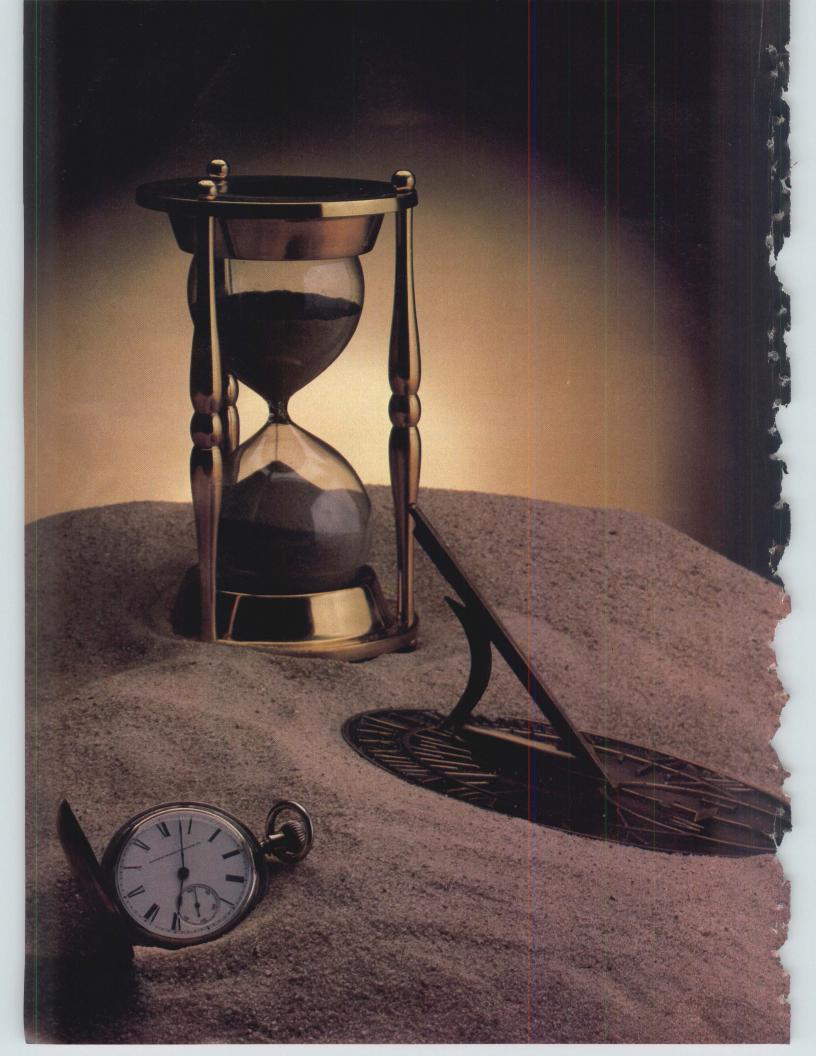
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LETTERS TO THE EDITOR

To the Editor:

I read David Townzen's article ("A Task-Scheduling Executive Program for Microcomputer Systems," June 1977, pp 194-202) with much interest. I did find a number of errors in the assembly listing. All these errors were due to the assumption that labels Q7OUT and BTBL7 will never be near a ¼k memory boundary. When incrementing pointers stored in double register (H,L), one should consider the consequence of a carry out of the most significant bit of register L.

The following four corrections should be added to the article.

1. ; COMPARE WITH INPUT POINTER INX H ; NOT INR L

2. ; GET TAG FROM QUEUE LOOKUP: INX H ; NOT INR L

3. ; GET ADDRESS FROM BRANCH TABLE

ANI TBLMSK ADD A XCHG

ADD L

JNC .+4 ; CARRY SHOULD BE CHECKED INR H ; AND ADDED TO H WHEN NEEDED

MOV L,A

4. ; LOAD TAG INTO QUEUE

INX H ; NOT INR L ADD L

JNC .+4 ; CARRY SHOULD BE CHECKED INR H ; AND ADDED TO H WHEN NEEDED

MOV LA

Correction

An instruction byte was inadvertently omitted from the listing of software for a 10-bit D-A converter display appearing on p 117 of the column "Microcomputer Interfacing: Using Digital-to-Analog Converters," by C. Titus, P. R. Rony, D. G. Larsen, and J. A. Titus, Computer Design, July

1977. Immediately following the MOVAM instruction at HI = 000 and LO = 011, the INXH instruction (043) must be inserted. All subsequent instruction bytes must be moved to the next higher address. The complete, corrected table is reprinted below.

Typical Software For a 100-Point, 10-Bit DAC Display

				*000 000	
000	000	041	START,	LXIH	/Load H & L with memory pointers
000	001	000		000	/LO address pointer
000	002	005		005	/HI address pointer
000	003	323		OUT	/Generate trigger pulse
000	004	007		007	
000	005	176	AGAIN,	MOVAM	/Get the first point
000	006	323		OUT	/Output eight LSBs
000	007	004		004	
000	010	043		INXH	/Increment the memory pointer
000	011	176		MOVAM	/Get the second part of the word
000	012	043		INXH	/Increment the memory pointer
000	013	323		OUT	/Output two MSBs
000	014	005		005	
000	015	323		OUT	/Strobe the DAC
000	016	003		003	
000	017	175		MOVAL	/Move L to register A
000	020	376		CPI	/Compare it to the data byte
000	021	310		310	/310 = 200 decimal
000	022	302		JNZ	/Done all 100 points?
	023			AGAIN	/No, do the next point by jumping
	024			0	/to again
	025			JMP	/Yes, jump back to start to do
000				START	/it all over again
000	027	000		0	

Other than these errors, I found the article to be very useful.

Jeffrey H. Lederer University of Pittsburgh Pittsburgh, Pa

The Author Replies:

Mr Lederer is correct in pointing out that the task-scheduling executive program assumes that the queue and branch table are each located within the boundaries of a 256-byte block of memory. The reason for this design is to minimize the execution time required to calculate addresses in the queue and branch table, since with this scheme the carry out of register L will never occur. The "fix" proposed by Mr Lederer, while removing the constraints on the location of the queue and branch table, adds an extra 15 to 22.5 ms (10 to 15%) to the execution time of the program. Since the task-scheduling executive program was designed for a real-time environment, a tradeoff of speed for memory allocation was chosen.

By the way, an additional "JNC .+4, INR H" is required following "ADD L" in the "Get Tag From Queue" section in order to make Mr Lederer's "fix" complete.

David A. Townzen Kaye Instruments, Inc Bedford, Mass

To the Editor:

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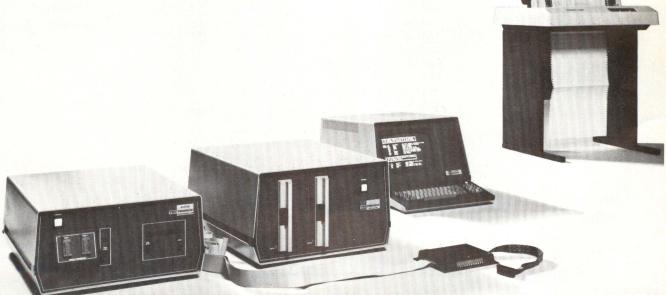
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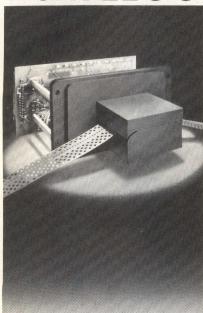
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To the Editor:

The ACM's SIGDOC group has started a review of the flowchart standard (ANS X3.5-1970). The committee seeks written comments and suggestions for the improvement, modification, or change of the current standard. Or, if there is no change appropriate at this time, please indicate so.

All types and levels of suggestions and comments are welcome. All concerned persons in the computer field are eligible. Send your written comments and suggestions to Ned Chapin.

Ned Chapin Flowchart Committee Chairman InfoSci, Inc Box 7117 Menlo Park, CA 94025

Letters to the Editor should be addressed:

Editor, Computer Design 11 Goldsmith St Littleton, MA 01460

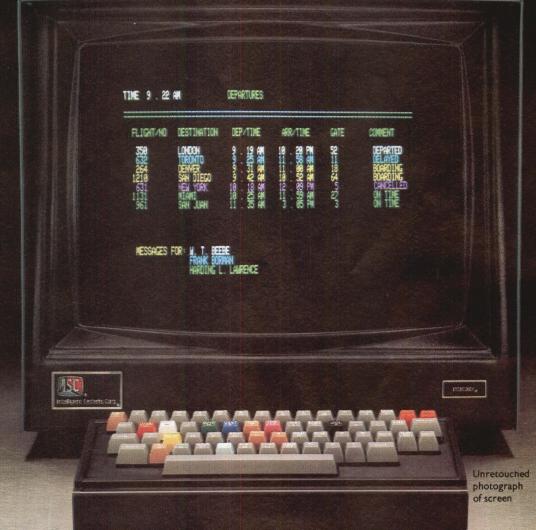
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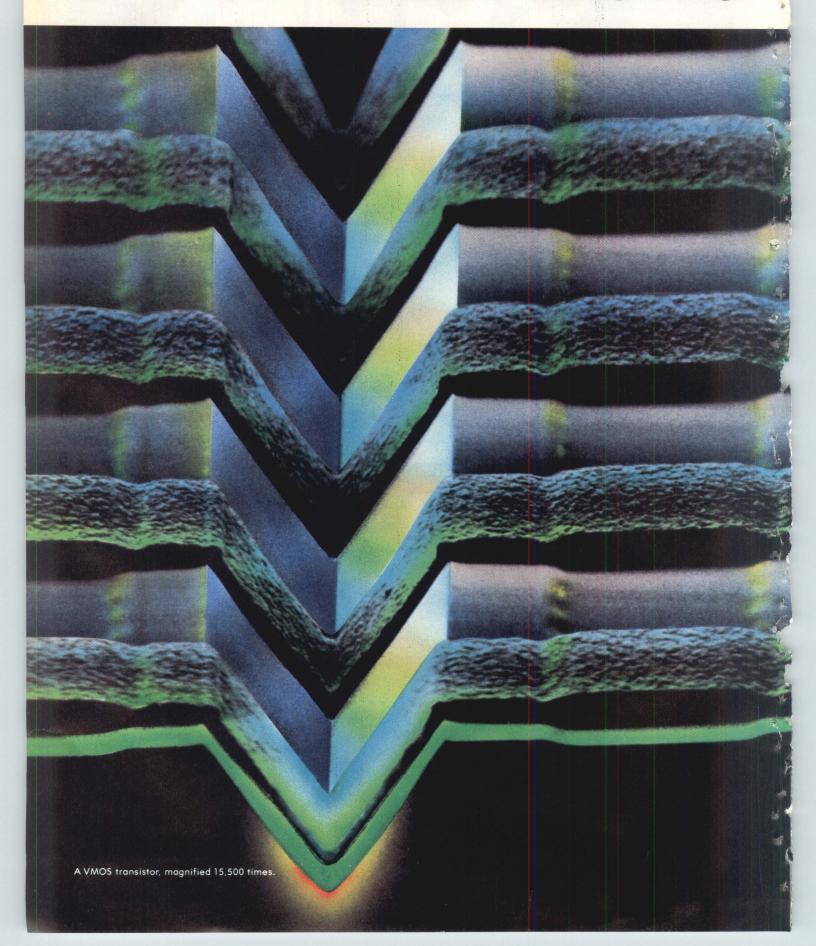
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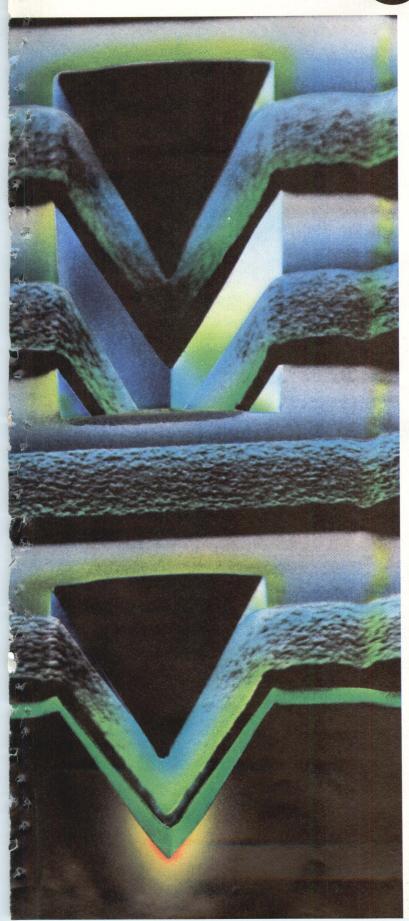
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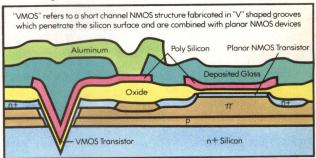
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CIRCLE 13 ON INQUIRY CARD

COMMUNICATION CHANNEL

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

System Environmental Factors

One of the primary causes of degradation and malfunction of a communications system is the environment. Concern for associated environmental factors is germaine to any electronic equipment. Normally, the central computer site—the system host computer—receives ample attention in this area. However, information communications systems which have distributed data terminals, concentrators, and remote I/O processors are commonly neglected; when the electronic device is located at other than the central site, environmental concerns often do not receive the same priority of attention.

Many times the actual manufacturer of such distributed equipment is the prime causal factor in this situation. In an attempt to present a product in the most attractive manner to a prospective customer, the manufacturer may encourage statements such as ". . . operates in a normal office environment" or ". . . no special installation needs, just plug it in like a typewriter." As a result, the user is lulled into thinking that the equipment has inherent immunity to its actual operating environment, while in reality it is highly susceptible to adverse environmental conditions.

A primary objective of design engineering is to produce a product that will function properly within set ranges of environmental conditions. However, too often the designer assumes that "normal office environment" support conditions will vary over known ranges—and that the system's design need only maintain stability within those ranges. In actuality this is only the first step. The designer must recognize that actual conditions will occasionally exceed nominal ranges.

Three major environmental conditions comprise the primary culprits. Temperature and humidity jointly rank as the leader in the field of potential system destroyers. However, while both work together to attack a unit of electronic equipment, temperature is the more significant factor with today's component technology. The second adversary is dirt and dust particles. Not usually considered, this cause can render the most subtle yet extensive damage to electronic equipment. The third and most immediate factor is that of primary power. Proper installation, power stability, and power availability must all be considered.

Temperature and Humidity

Adverse temperature as evidenced by extreme heat or cold can cause a myriad of component weaknesses. All manufacturers specify an acceptable operating temperature range for their equipment. Unfortunately, most users consider operating temperature as a factor only

when the equipment is in use; they are not concerned with environmental temperatures when the equipment is dormant, such as during night hours or weekends. However, the fact that equipment is powered creates the same susceptibility to temperature extremes as when it is functioning.

With today's energy concern it is not unusual for management of commercial buildings to change temperature thresholds for air conditioning and heating systems during night hours, or to totally deactivate the systems (particularly air conditioning) during weekends. As a result, the ambient temperature degrades to the point where circuit damage will inevitably result if the equipment is kept in a powered condition.

Typically, the mean-time-between-failures for a given component will be reduced by 50% for every 10 degrees above the normal recommended operating temperature. The differential between room temperature and the temperature at the top of an electronic equipment cabinet is usually 10 to 15 degrees. A minicomputer-based system with memory and associated electronics easily achieves a 15- to 20-degree differential. If that equipment is located in a room that on weekends reaches 95 to 100°F due to air conditioning shutdown, the cabinet temperature can approach 115 to 120°F. Although not in use, the system's being powered results in the same degradation and, eventually, permanent damage. Such a situation typically results in highly error prone operation on Mondays and ultimately random and seemingly unrelated circuit failures.

The user must be fully aware of all possible environmental extremes. If such conditions are possible, the equipment must be powered down during such potential periods, or auxiliary air conditioning or heating equipment provided. It is also very important that a record of past temperature extremes be maintained, with room and cabinet temperatures simultaneously monitored. A temperature chart recorder should note both temperatures; even inexpensive maximum-indicating thermometers are effective if read and reset on a frequent basis. Ideally, a temperature threshold alarm system for unattended equipment would alert personnel when preset temperature conditions are reached.

Humidity is not a major factor until condensation begins or the saturated air coupled with dirt and dust particles begins to exhibit a conductivity characteristic. Physical damage such as warped printed circuit (PC) boards is virtually nonexistent. Continued high humidity, approaching jungle conditions, will naturally result in





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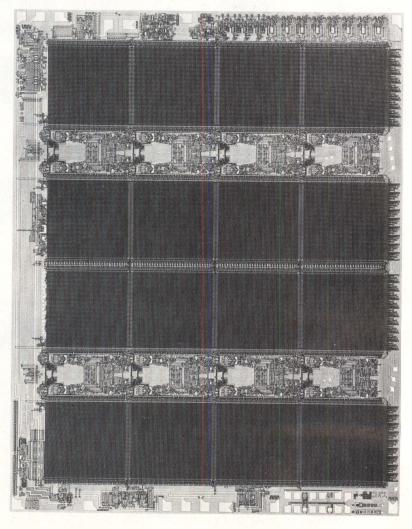
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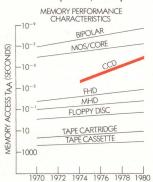


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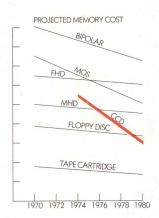
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fungus growths that will rot the equipment. Fortunately, such an extreme is not often found in today's commercial and business environments.

Dirt and Dust

A high dirt or dust environment will first become evident in the filters, hopefully installed by the manufacturer at the equipment cabinet blowers. Frequent inspection and cleaning of these filters not only will insure that dirt and dust particles do not reach the electronic components, but also will provide for free air flow through the equipment. If the internal air flow is impeded, the temperature differential will increase dramatically. A moderately dirty filter could easily raise the differential over 30 degrees.

Under extreme conditions, high humidity coupled with a dusty or dirty atmosphere can produce a conductive solution that condenses on various electronic components, causing a component to literally destroy itself. For instance, an electronic system that experienced chronic failures was found to have a virtually imperceptible coating of "dust" on each PC board. Subsequent tests showed that this coating had sufficient conductivity characteristics to have allowed internal signal distortion and leakage.

However, unless the environment is likely to be highly polluted, the use of particle detectors is rarely justified. Isolation of equipment in a closed room with directly filtered air outlets or vents is ample precaution. Frequent cleaning or replacement of these filters as well as those within the equipment is adequate basic protection. As a secondary precaution, care should be taken that personnel with access to the equipment or



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to the area are not carriers or producers of adverse dust or dirt particles.

Primary Power

The first major concern of primary power is proper grounding of the circuits, which is the most common cause of system malfunctions if done improperly. While this may seem self-evident, it is not unusual to find a significant potential existing between the primary power neutral lead and the actual frame ground. It is normally assumed that within a building's electrical distribution system this interconnection is properly maintained. Yet, in a multistory building, a significant difference can develop. In a recent experience, when a minicomuputer's magnetic tape peripheral was turned off, the minicomputer's memory information was mutilated. A potential of over 56 Vac was measured between ground and the primary power neutral. In effect, the system was "floating," inviting any kind of spurious power signal to invade the primary system. The assumption that the primary power was properly terminated and would maintain that termination led to this failure.

Virtually every well-designed power supply will compensate for nominal power fluctuations. Unfortunately, it is not unusual to have relatively common power variations that exceed the tolerances of the equipment's power supplies. In such environments auxiliary primary power regulation equipment, which is relatively low cost, should be installed at all equipment sites which have unattended and/or multiple device dependency, such as remote concentrators or remote I/O processors. This level of precaution is usually not warranted at a remote interactive terminal; yet it may be necessary at a remote job entry (RJE) terminal site.

If actual power outages are a reasonable, or even remote, probability, and the associated application's operational sensitivity is totally intolerant of such outages, an uninterruptible power supply (ups) must be considered. Normally not a remote terminal installation consideration, ups may be a vital necessity at a concentration location as well as at a primary processing site. Economic factors heavily influence a ups decision; a minimal 7.5-kVA system with 8-h capacity will require an investment of approximately \$20,000. While also providing the function of auxiliary power regulation, the ups has a cost almost two orders of magnitude greater than basic auxiliary power regulation.

If a UPS is to be implemented, care should be taken to include all critical system equipment and devices. A classic example is a remote I/O processor that utilized dial access communications with its localized remote terminals. Since the modems were not provided by the local telephone utility, connecting arrangements were installed. The UPS successfully maintained operations between the remote I/O processor and the host computer in a subsequent power failure. Unfortunately, the fact that the connecting arrangements were also ac powered had not been considered. As a result, the viable remote I/O processor was unable to communicate with its localized remote terminals.

The major source of frustration is that the impact of these environmental factors is appreciated only after the damage has been done. In retrospect the proper attention to these matters would have been relatively easy, incurring only minimal cost. The finest designed equipment can be reduced to valueless junk by an improper operating environment. This process of degradation occurs subtlely while at the same time causing randomized, unrelated component failures and system errors which are dismissed as being the result of alleged poor equipment design and engineering.

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second board gives you the advantage.

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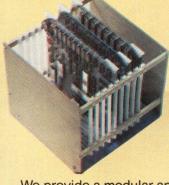
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- Z80-PMB PROM Memory Board: Contains sockets for up to 32K bytes of EPROM or PROM and additional programmable I/O channels.

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- Z80-SIB Serial I/O Board: Provides additional four (4) serial duplex channels.
- Z80-VDB Video Display Board: Interfaces the MCB to a standard video monitor. This board contains 256 bytes of memory and also interfaces to a ASCII standard keyboard.

versatility of attack: you can buy only as much as you need.



We provide a modular approach to complete computing and processing systems. Zilog products are available as a basic CPU card, a card set or a complete self-contained computer with floppy disks.

Behind all this is Zilog's pledge to stay a generation ahead. We're the specialists who are responsible for the development of the most successful first and second generation microprocessors.



CIRCLE 17 ON INQUIRY CARD

Zilog

10460 Bubb Road, Cupertino, California 95014 (408) 446-4666/TWX 910-338-7621

EASTERN REGION: (617) 890-0640 MIDWESTERN REGION: (312) 885-8080 WESTERN REGION: (213) 540-7749 EUROPE (ENGLAND): (0628) 36131/2/3

AN AFFILIATE OF EXON ENTERPRISES, INC.

Series 1 users can now add mag tape memory capability to their Series 1 (Models 3 or 5) installation! The new DATUM seven- or nine-track system permits recording densities of 200 bpi NRZ through 1600 bpi, phase-encoded. Speeds: from 12.5 ips through 125 ips. As many as four transports can be used.

Individually driven tape drive I/O ports. Read-after-write parity checking. Quartz-crystal-generated timing. Interfaces to industry-compatible drives.

The system incorporates the new DATUM "Universal User's Adapter," a device that allows connection of external devices to the Input-Output bus of Models 3 or 5 of

New! the IBN
DATUM
Tape
System in
for
IBM
Series 1!

the IBM Series 1 computers. The Adapter operates in the "cycle -steal" mode while exchanging 16-bit words with the computer. With this Adapter, Series 1 users can tailor their system to their own exact requirements, even to the extent

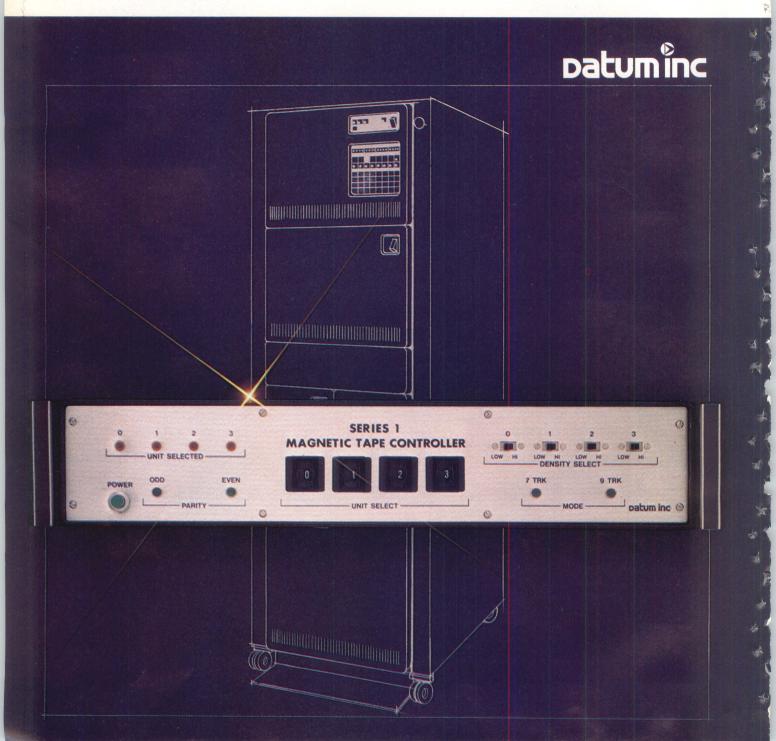
Diagnostic and operational software is included with each system. Color-coordinated cabinets can be ordered. Service and installation are offered throughout the U.S. Deliveries are 90 to 120 days ARO.

of interconnecting several computers.

CIRCLE 18 ON INQUIRY CARD

Peripheral Products Division 1363 S. State College Blvd. Anaheim, California 92806 TWX: 910/592-1289 • 714/533-6333

Telex 68-5579



Added Model and Pricing Adjustments Enhance Computer Series

To bring greater cost-effectiveness to the communications-oriented small-to medium-scale computer systems market, Burroughs Corp, Detroit, MI 48232 has announced price reductions of 25 and 15% respectively for purchased and leased B 1800 and 1700 models, and 50 and 30% for add-on memories. Computer periph-

eral equipment prices are also adjusted. All lease rates include 24-h/7-day field engineering availability.

An additional model, the B 1720-1 computer system is designed for online data entry, online programming, remote job entry, and other data communications functions. The system features a 6-MHz cpu, 98k bytes of main memory, 4k bytes of control memory, console, 87M-byte disc pack, 400-line/min printer, and communications control.

Circle 400 on Inquiry Card

1600 Series Video Terminals Are Selected for CALRS System

R W

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P

The Centralized Automated Loop Reporting System (CALRS) has been installed in Hamilton, Ontario, Canada with 1600 series video terminals from Westinghouse Canada Ltd, PO Box 510, Hamilton, Ontario, L8N 3K2 Canada providing the communications interface between service personnel and the system's computers. The interactive W1600 terminals

allow service operators and repair technicians to access the system's three PDP-11/40 minicomputers to initiate automated diagnosis and correction of customer problems with telephone equipment. Developed jointly by Northern Telecom Ltd, Bell-Northern Research, and Bell Canada, the system uses minicomputer technology to store and retrieve information, and to perform up to 15 measurements plus operating checks to diagnose faults in customer equipment.

Protocol Links PDP-11 Computers to Datapac Network

SNAP (Standard Network Access Protocol) will interface the line of computers from Digital Equipment of Canada, Ltd, Kanata, Ontario to the Datapac network of the TransCanada Telephone System. Known as X.25, the protocol has been ratified by the CCITT as the international standard for accessing public packet networks in the packet mode. The interfacing of PDP-11 computers with the network is aimed at rapidly and economically distributing information between remote sites.

Microwave Radio and Multiplex System Features Six T-1 Line Capacity

Operating in the 2-GHz common carrier band, the DRM2 integrated digital microwave radio and multiplex system offers 50% more channel capacity by increasing the "bits/Hz" density of the bandwidth through the use of raised cosine filters and a 4-level quadrature amplitude modulation technique. In addition to six T-1 (or DS1 line capacity), the system from TRW Vidar, 77 Ortega

Ave, Mountain View, CA 94040 features four auxiliary vF (voice frequency) channels in addition to an order wire and alarm channel.

Circle 401 on Inquiry Card

Light Source for Fiber Optic Systems Uses Silica Core Cable

A rugged PFX silica core fiber optic cable manufactured by DuPont Co, Wilmington, DE 19898 is being used to form the pigtail of an RCA-developed fiber optic light source. The high speed GaA1As in emitter (C30133) offers high speed response to electrical input signals up to 150 MHz at 820 nm. RCA has prealigned and permanently adhered the PFX-S120R cable in the precise position to couple the maximum signal from the device.

With a calculated numerical aperture of 0.43, the cable allows up to 18% of available energy to be coupled into the fiber and transmitted out the end of the pigtail. The emitter launches typically 150 μW out the end of the fiber, and is ready to be attached to the rest of a fiber optics system with any of several cable connectors presently being developed. Plastic-clad PFX-S cable has inner and outer jackets of the company's Hytrel polyester elastomer, with Kevlar aramid fiber, providing tensile strength in excess of 65 kg.

Expansion of Dataphone Digital Service Adds 30 Metropolitan Areas

In a filing with the Federal Communications Commission, the American Telephone and Telegraph Co, Long Lines Dept, Bedminster, NJ 07921 has proposed to expand its Dataphoneⁿ digital service to 30 more metropolitan areas, bringing the total to 96. The company requested authority to construct and operate the expanded network in order to meet the demand for digital services. The service provides end-to-end digital data transmission at speeds between 2400 and 1.544M bits/s.

1M-Hour Lifetimes Are Predicted for Solid-State Lasers

Results of long-term accelerated aging tests on solid-state lasers being evaluated by Bell Telephone Laboratories, Research and Development Unit of the Bell System, Mountain Ave, Murray Hill, NJ 07974 for lightwave communications systems indicate that average projected life-

The 2900 Family: Two years later.

1975. Advanced Micro Devices introduces the world's best 4-bit microprocessor slice, the Am2901, along with a few support circuits.

1977. It's a whole new family. Now there's an Am2901A just like the Am2901, only better. Now there are 18 support circuits, two or three second sources and all the software you'd ever want. The 2900 family has become the family of the future. Here's why:

The first family.

The Am2900 family is the first group of products designed specifically for microprogrammed machines. Microprogramming is rapidly becoming the most popular way to design medium- and high-performance systems, to reduce development time, make changes easily, and conveniently add new features.

Less weight, less size.

With the Am2900 family, it's not uncommon for entire boards to be eliminated. You'll shrink system size and weight, increase

overall reliability and reduce manufacturing costs.

Time goes by, price goes down.

In July 1975, we told you we'd reduce the cost of the Am2901 by 30% per year. We've done it twice. Once in April 1976 and once in March 1977. The Am2900 family gets less and less expensive all the time.

We're so popular, we're the industry standard.

The Am2900 family is the most widely used Bipolar LSI family in:

- Minicomputers: For emulators, high-performance CPU's and add-ons by eight out of the top ten U.S. manufacturers.
- High-performance controllers: For discs, tapes, floppy discs and universal controllers.
- Communications: For PBX systems, central exchanges, multiplexers and modems.
- Military: For radar processors, display systems and the Navy's new standard avionic computer, the AN/AYK-14.

The Family:

CPU Slice (ALU and general registers)

Microprogram Control Units

Branch and Instruction Control for Microprogram Sequencers

LSI Bus Interface Devices

Priority Interrupt Control

Main Program Control
New More Powerful MSI

functions

*In Development

Am2901A, 2902, 2903* 2904*

Am2909, 2910,* 2911 Am29803, 29811

Am2905, 2906, 2907, 2915A, 2916A, 2917A

Am2913, 2914

Am2930* 2931* 2932*

Am2918, 2919, 2920 2921, 2922

Plus:

Schottky and low-power Schottky MSI, MOS static and dynamic RAM's and all the devices you need to build your high-performance microcomputer.

We don't sell and run.

Advanced Micro Devices offers learning aids to help speed up designs and keep your engineers up-to-date on the very latest microprogramming techniques. Learning aids and application materials like these perennial favorites:

- A 16-Bit Microprogrammed Computer
- The Am2900K1 Learning and Evaluation Kit The Microprogramming Handbook

- A High Performance Microprogrammed Disc Controller In development:
- Vertically Microprogrammed State Machines
- An emulation of the Am9080A/8224/8228 using the Am2900 family

And two terrific design aids:

AMDASM

Our powerful, easy-to-use microprogram assembler offering software support through the worldwide INFONET time-sharing division of Computer Science Corporation. (It supports user-defined mnemonics for producing microinstructions up to 128 bits wide, and includes formating and default features as well as tape generation for PROM programmers. If you've got the other guy's MDS system, ask for AMDASM/80. It comes on a floppy disk and runs under their operating system.)

AMDS

Beginning this fall, we'll be offering hardware support with the Advanced Microprogram Development System. (It's the first prototyping system especially designed for microprogramming systems.) It'll help speed up construction of prototype systems and generation and de-bug of microcode. Resident AMDASM, of course!

The Am2900 family.

It's today's product family for tomorrow's high-performance machines. Am2900. Remember that number. You're going to be hearing it a lot.

Advanced Micro Devices

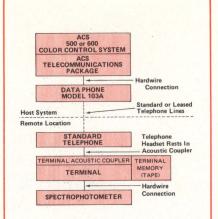
Bipolar LSI. N-channel, silicon gate MOS. Low-power Schottky. Multiple technologies. One product: excellence.



times are 1 Mh, or 100 yr. Groups of lasers were operated at higher than room temperatures (90, 70, and 50°C) causing them to fail in measurable times. The high temperature results were then extrapolated to lower temperatures to project room temperature (22°C) lifetimes. Since equipment frame temperatures in operating lightwave systems exceed 22°C, thermoelectric cooling devices will be used initially to maintain near room temperature conditions for the lasers.

Package Provides Color Control Capability for Remote Locations

For installations with limited color control requirements, Applied Color Systems, Inc, PO Box 5800, Princeton Service Center, Princeton, NI 08540 has introduced a telecommunications option providing remote site operators with use of the company's 500 or 600 system and the full



Connection between Applied Color Systems' 500 or 600 color control system and components of telecommunications option at remote location

Chroma-Pac software library. A color measuring spectrophotometer, appropriate computer terminal, and tele-

phone equipment are required to use the package at a remote site. The systems are used in textile, paint, plastics, ink, and printing industries. Circle 402 on Inquiry Card

1200-Bit /s Modems Are Installed in Singapore **Communications Systems**

To meet multi-year requirements, the Telephone Authority of Singapore has begun to install the first of 300 1200-bit/s modems in its communication systems. In either standalone or rack-mount versions featuring LSI circuits and asynchronous operations, the modems, manufactured by General DataComm Industries, Inc, 131 Danbury Rd, Wilton, CT 06897, were sold and delivered through the company's area distributor, International Aeradio Ltd, Singapore. As part of the program, the company is training Telephone Authority personnel in equipment operations and maintenance.

Ironless Core Micro Motors (Tachometers).



35mm of instantaneous power. Featuring long life carbon brushes, ball bearings and our unique hollow rotor to provide you with low noise, high efficiency and coggless performance. Hitachi also makes a full line of ironess core micromotors: 17, 22 and 26 mm diameter series. These motors are precision made with our patented precious metal wire brush system (eliminating brush bounce) Commutators are made of precious metal also, giving maximum life and high reliability for your product. You can't Swiss miss. Special shafts, ball bearings, and modified windings are available to accommodate virtually any specific applications.

THE CHI HITACHI HITACHI

DC Permanent Magnet

Motors. (Also available with our incremental encoder complete and assembled.)



Our DC permanent magnet motors have pleased many of our customers in such varied places as printer carriage drives, duplicating machines, x-y axis control drives and high density magnetic tape transports. We can satisfy your application requirements too with one of our various rotor designs or high performance low inertia motors. All are available with our incremental encoder integrally mounted, completely assembled, tested and ready for your immediate installation.

For more information, contact: Hitachi America Ltd., 100 California Street, San Francisco, California 94111. (415) 981-7871 Bill A. Mahoney

Fractional Horsepower Fractional Horsepower **AC Induction Motors.**



Various designs of these motors are used for several applications such as: spindle drives, disc pack drives, fan drives and many others.

Hitachi can be used as your single source for virtually all of your motor requirements. This facilitates easy coordination, with one vendor, for procurement of several types of special motors without the difficulty of working with many companies for each type of special motor. Hitachi accomplishes this by widely diversifying its large motor manufacturing facilities.

Quality always comes first at HITACHI



"New cost/performance analyses made Inforex switch from in-house tape drive production to Digi-Data" DAVID I. CAPLAN — INFOREX VICE President, Engineering

Although once a strong believer in vertical integration, Inforex no longer makes the synchronous tape transports used in several of its system designs, including the new System 7000 Distributed Data Processing System. The reason: a thorough analysis indicated that leading-edge tape transport equipment costs Inforex far less from Digi-Data

than when we had to design, manufacture, inspect and inventory it ourselves.

Cost wasn't the only make/buy factor, however, even though Digi-Data prices are 20-40% lower than its leading competitors. System 7000 needed an advanced tape drive that would handle magnetic tape accurately, gently and with ultra-reliability. Inforex found that Digi-Data's features including ease of maintenance and simplicity of design could deliver that value combination.

Equally important, Inforex was freed to focus its own resources directly on total data entry system development. They know that staying current in tape transport technology is what Digi-Data does best. And like many other OEMs, they've found that taking advantage of it helps their customers.



DIGI-DATA CORPORATION

8580 Dorsey Run Road, Jessup, MD 20794 (301) 498-0200

... First in Value!

CIRCLE 20 ON INQUIRY CARD

We've combined refresh with storage in a new modular graphics display.

You build from there.

Suddenly state-of-the-art display technology comes built for the OEM.

Tektronix' new GMA display modules let you integrate into your system our most impressive display capabilities ever. Including refresh and storage graphics in one tube. Complete character and vector generators. Big 19" screen and fine resolution.

It's exactly what you need, because you can specify exactly what you want. Order CRT and power supply only, or select from a range of performance and packaging options in our extensive product line. You can integrate other products from our graphics family, like hard copy modules. Or talk to us about other special product configurations, like our 11" storage-only components.

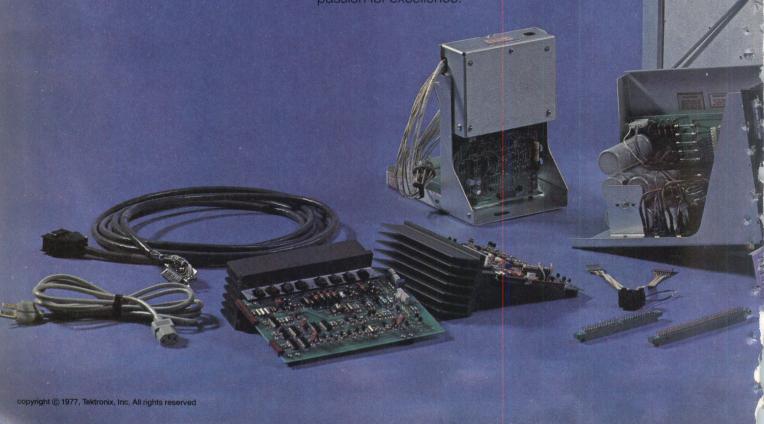
No other package lets you pick such comprehensive graphic display capability at anywhere near the price.

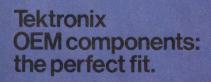
It figures, because Tektronix has been the worldwide low-cost graphics leader for years. No matter what unique and unusual systems you're working with, we can help with manufacturing flexibility, engineeering assistance, and a passion for excellence.

Get capability you can build with. From a supplier you can work with. Get your Tektronix OEM Sales Engineer on the phone today. Or write us for more information.

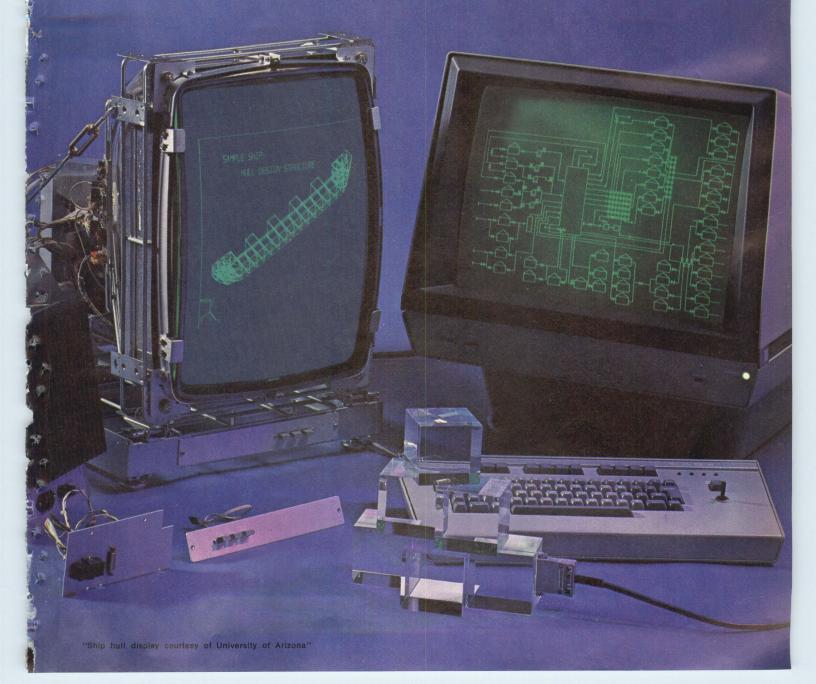
Tektronix, Inc. Information Display Group OEM Components P.O. Box 500 Beaverton, OR 97077

CIRCLE 21 ON INQUIRY CARD







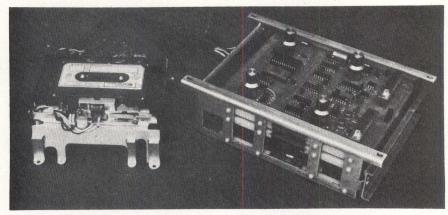


DIGITAL TECHNOLOGY REVIEW

Microprocessor Control Adds Versatility to Cassette Recorder

STR®-300 is a microprocessor-controlled cassette recorder which offers a cost-effective solution to program storage, program loading, and/or retrieval requirements in system applications. Complete with a serial 1/0 interface that receives or transmits eight bits of serial data and is RS-232-C or 20-mA current loop compatible, the unit requires only a power supply and mounting location to become completely operational. A briefcase version of the unit, the STR-Link II (see Computer Design, Aug 1977, p 152) is also available.

Electronic Processors, Inc, 1265 W Dartmouth Ave, Englewood, CO 80110, designed the unit with an internal microprocessor which controls data flow, I/O control signals, and tape transport and control character decoding. This adapts the device to use as a transparent storage medium

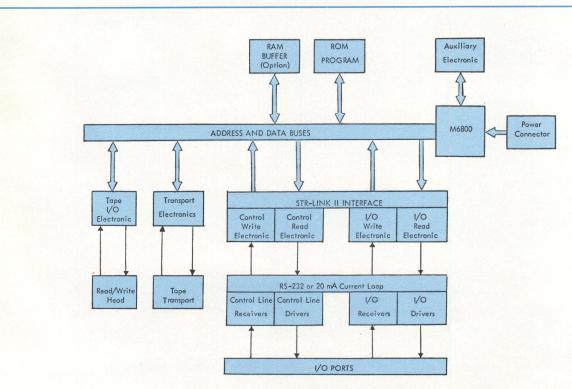


Electronic Processors' cassette recorder controls transport functions with a micro-processor to provide reliable program storage and loading, and data retrieval with devices requiring remote control of the tape drive

in serial interfaces (RS-232, 20-mA current loops), and as a paper tape replacement in applications such as teleprinters. An optional RAM buffer enables read and write operations at different speeds (110 to 9600 baud); another optional buffer allows incre-

mental operation, data compaction, peak rate of 9600 baud, and variable record length.

Both 1/0 ports have 20-mA current loop interfaces for bidirectional data transfers. Remote control of the unit through these interfaces can be ex-



STR-300 cassette recorder uses a microprocessor to control data flow, I/O control signals, tape transport, and control character decoding, for high data reliability with low cost digital cassettes. Unit is complete with serial I/O interface that receives or transmits eight bits of data and is RS-232 or 20-mA compatible





Data General. A la carte.

Now, you can buy our DASHER™ terminals, even if you don't own a Data General computer system. Select our fast impact printer and our user-oriented video display. Both are interface-compatible with any standard computer system.

Choose either 60 or 30 cps versions of the DASHER printer, which has a standard typewriter keyboard, u/l case, 132 columns.

DASHER display features a 1920 character screen, u/l case, convenient detached keyboard, programmable function keys, and a monitor that tilts and swivels.

Just as DASHER terminals' features make them easy to use, their attractive appearance makes them

easy to fit into any environment.
And of course they are solidly reliable and easy to maintain, a Data General trademark. For more details call your Data General sales office or nearest independent supplier of Data General terminals. Or send the coupon. Even a bit of Data General in your computer system is better than none.

I'm interested in					terminals.
	no.		type		
Name					1
Title					
Company					
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City		State		_Zip_	
Mail to: Data General					
DASHER is a trademark of Dat					CD-9

Data General

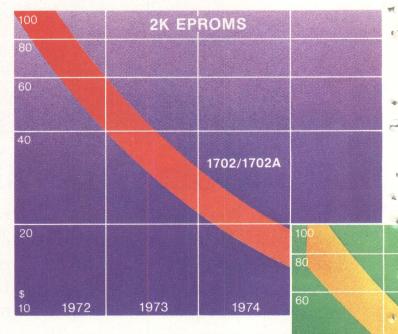
It's smart business

Data General, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario. Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361.

Intel delivers the best for today

Industry standards, volume support and cost efficiency are what you've learned to expect from Intel, the company that invented EPROMs and delivers more of them than all other manufacturers combined.

In 1972 we introduced the world's first EPROM, the 2K 1702. Then in 1975 it was the 8K 2708 which quickly became the industry standard. Now we're delivering the 5 volt 2716 EPROM with the performance and economic advantages it takes to be the industry standard 16K EPROM—for today's system upgrades from 8K to



16K and for tomorrow's systems designed with 5 volt microprocessors.

For economy, the 2716 offers a die size 20% smaller than any other 16K EPROM and a price-volume learning curve that will descend even more rapidly than our 1702 and 2708 EPROMs. And the 2716 is the only 16K EPROM with a pin for pin interchangeable 16K ROM, the 2316E.

For performance, the 2716 consumes a maximum of 525 mW in the read mode. That's 50% less power than our 2708 and 25% less than any other 16K EPROM. Intel's unique power-down feature reduces the standby current to 25mA maximum, a 75% savings over active power. And at 450ns there's no penalty in access time.

Programming the 2716 is simpler and twice as fast as any other 16K EPROM. Single-pulse, single-location

PART	SIZE	POWER SUPPLY	MAXIMUM	CURRENT	ACCESS TIME (MAX)	COMPATIBLE ROM
NUMBER			ACTIVE	STANDBY		
1702A	256 x 8	+5V -9V	65 mA	65 mA	1 μs	1302
2708	1K x 8	+5V -5V +12V	10 mA 45 mA 65 mA	10 mA 45 mA 65 mA	450 ns	2308
2758	1K x 8	+5V only	100 mA	25 mA	450 ns	2316E
2716	2K x 8	+5V only	100 mA	25 mA	450 ns	2316E



40

20

8K and 16K EPROMs and tomorrow.

programming and TTL-levels allow programming onboard, even in the field. Use the Intel Universal PROM Programmer or any other commercially available programmer to program any 2716 word location, either individually, sequentially or randomly.

Intel's 2716, along with the compatible 2316E ROM, is your best choice for upgrading from 8K to 16K.

8K EPROMS

2708/2758

For new designs using 5 volt microprocessors, the 2716 and new 5 volt 2758 8K EPROM are the obvious choices.

The 2758 is the lowest power 8K EPROM available. Use it for small systems where 1K bytes is all you need, or for 1K byte modularity. The 2758 has all the cost savings and performance benefits of the 2716. And since the 2758 and 2716 are completely interchangeable, future upgrading from 8K to 16K in 5 volt systems is simplified.

Go with Intel industry standard EPROMs because they give you maximum value in today's system upgrades to 16K and in tomorrow's 5 volt designs. Order the 2716, 2758 and

compatible 2316E ROM from your Intel distributor.

For technical information and a copy of "The new 16K EPROM" article reprint (AR-42) write Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051. In Europe contact Intel International Brussels, Belgium. Telex 24814. In Japan contact Intel Japan, K.K. Tokyo Telex, 28426.



intel delivers.

ercised via control characters. Current loop operation of the data terminal port is limited to 110 baud; the data set port can operate at 1200 baud unbuffered, or up to 9600 baud buffered.

Data transfer characteristics are established by setting four front panel switches. Baud rate is set via an 8position rotary switch which fixes data transfer rate at 110, 150, 300, 600, 1200, 2400, 4800, or 9600. A 2-position stop bit switch selects either one or two stop bits in the data character format. Half- or full-duplex mode is selected using the 2-position mode-select switch. In half-duplex mode, data transfers can be made from both 1/0 ports. In full duplex, the tape device is visible only to data transfers to or from the data set interface port.

The type of interface is determined by manipulating the 3-position I/o select switch: RS-232 setting engages both I/o ports in the RS mode; current loop online disables the RS interface and enables the current loop at both I/o ports; and current loop local totally disables the data set interface port, and enables the 20-mA current loop at the data terminal interface port.

Standard Philips digital cassettes serve as the storage medium; a bit-serial speed tolerant recording technique assures data integrity. The technique records approximately 92k 8-bit characters on one side of the tape. Recording speed is 5.5 in/s (14 cm/s); rewind speed is 100 in/s (254 cm/s).

Circle 140 on Inquiry Card

4-Color Graphic Plotter Uses Microprocessor to Enhance Efficiency

Microprocessor-based circuits in the 7221A flatbed plotter improve operating efficiency to reduce timeshare computer and transmission costs. Among the features of the 4-color graphic plotter are built-in buffer memory, internal alphanumeric character generation, internal arc and circle generation, and user-defined dashed line patterns. Any sequence of plotter instructions can be stored in the buffer memory as macroinstructions for recall; up to 64 different macroinstructions can be stored at one time.

Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, in designing the machine, combined firmware with software to offer sophisticated multicolor hardcopy graphics plotting from remote facilities at low communications costs. Equipped with a standard RS-232-C asynchronous interface (CCITT V.24), the plotter operates from 75 to 2400 baud, halfor full-duplex and can plot data from its 1150-char buffer while the computer and terminal are used for other tasks. An additional 2048 characters of buffer memory is available as an option.

Color graphics are achieved through programmable pen changing. The plotter automatically selects any of four pens under program or front panel control. Pen changing is accomplished using only the normal pen moves; no additional motors or solenoids are required. Manual pen changing is not required.

Each pen is stored in its 'stable' and is picked up by the plotting arm under program or front panel control. When a pen is returned to the stable it is capped to prevent drying. Pen velocity can be varied in 1-cm/s increments from 1 to 36 cm/s maximum under program control.

Among the unit's special features are an internal character generator containing six fonts including common European, special mathematical, and graphic symbols. Alphanumeric characters are created with a single command. Character plotting speed is typically three 2.5-mm char/s.

Plot resolution is programmable to 0.025 mm. Line quality is achieved by a motor control technique which provides control to 0.008 mm at the full pen speed of 36 cm/s. Plotting accuracy is $\pm 0.2\%$ of deflection length, ± 0.2 mm. Repeatability is 0.04 mm with any one pen, or 0.2 mm with multiple pens.

Users can define any sequence of up to 32 dashes and spaces, and all lines and circles will be drawn in the defined style. A single command defines a circle in either direction at any radius. Angles of rotation can be specified to any desired angle with up to 0.06-deg resolution.

Price of the 28 x 40 cm flatbed plotter is \$4600; the expanded input data buffer sells for an additional \$225. High level fortran subroutines are available for HP 1000 and 3000 series computers and for several commercial timeshare services.

Circle 141 on Inquiry Card

Word Processors Include Shared Logic Software for Multiterminal Networks

A family of video display text editing systems, based on the WT78 video display terminal, range from single-user standalone systems to multi-user information processing networks. Shared logic software makes disc storage as large as 88M bytes available to as many as 48 users. Communication capability allows individual units to interact with each other or with a central processor.

Principal component of the systems, from Digital Equipment Corp, Maynard, MA 01754, is the WT78, a low cost word processing terminal with 1920-character display and an Lsr version of the PDP-8 with 16k words of memory (see Computer Design, July 1977, pp 30, 35). The integrated video terminal/processor manages text entry and editing in a variety of configurations.

A single-user system, the standalone WS78 consists of WT78 terminal, floppy disc unit for local mass storage, and either a letter quality printer or LA78 180-char/s matrix printer. Using WPS-11M software, the WT78 can interact with PDP-11 systems to form multi-user information processing networks.

The WPS-11M software package provides multiterminal word processing capabilities for PDP-11 computers using the RSX-11M real-time operating system. The package permits a word processing system user to have access to full storage capabilities of the computer as well as to establish distributed word processing operations from a central computer system.

Up to 48 WT78 terminals or WS78 stations may be linked to an 11/70 processor. By using the built-in minicomputer in the terminal, the central processor can operate in parallel with word processing operations at individual stations, permitting maximum use to be made of both terminals and central computer. Terminals retain full editing and word manipulation capabilities, allowing users to prepare and edit reports, communicate drafts to other word stations or terminals, and output to either a letter quality printer or high speed printers. Circle 142 on Inquiry Card

High Performance Models Added to Family of Medium Scale Computers

Compact, high-performance models B 2810 and 2815 are designed for ef-



Matrix Horsepower



A 100% Duty Cycle Makes Ours The Workhorse of Matrix Printers!

Inherent Diablo ruggedness and reliability and our unique ballistic head design give our Matrix printer a 100% duty cycle. Add to that, bidirectional printing,

high speed tabbing, skip-over spacing and vertical forms control and the result is greater throughput. Our wide-gap ballistic head means paper clearances are never a problem and field head change requires only an allen wrench — no alignment! (All this plus incremental printing capability

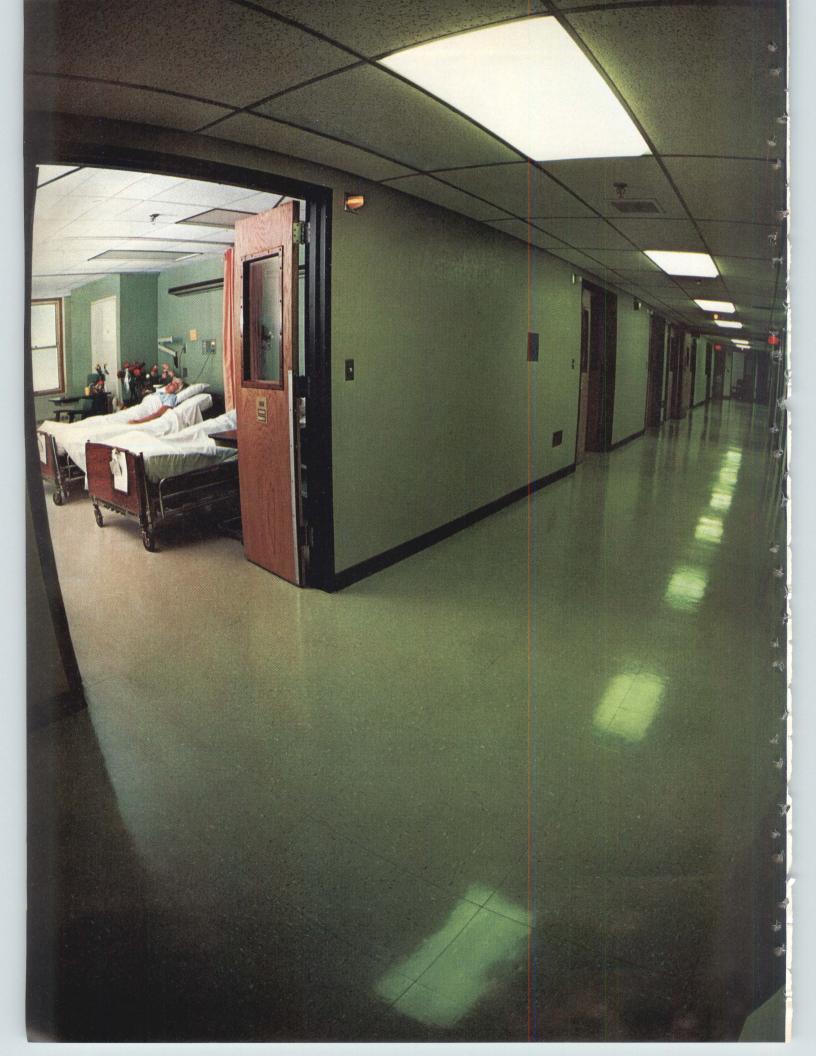
make our printer an ideal component for a workhorse terminal.) For a complete product demonstration, Diablo Systems, Inc., 24500 Industrial Blvd., Hayward, California 94545, Diablo Systems, S.A., Avenue de Fre 263, 1180 Brussels, Belgium, or Mitsui & Company, Ltd., 2-1 Otemachi 1-Chome, Chiyoda-ku, Tokyo.





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The quickest way to find a nurse is to ask an LSI-11 microcomputer.

When GTE Sylvania was looking to design the most advanced computerized hospital communications system in the market, they looked no further than our LSI-11.

The LSI-11 is the highest performance, most softwaresupported micro device you can buy.

Which is why some people think that the LSI-11 may be just a bit too much.

Yet for lots of applications — like Sylvania's — anything less than the LSI-11 isn't really enough.

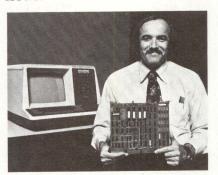
GTE Sylvania's System
Twenty-One is designed to
handle all nurse/patient communications in a hospital
through one central operator
using a Sylvania-modified
Digital VT52 CRT terminal as a
Central Console. The idea
behind it is to allow nurses
more time for nursing by freeing them from handling calls,
while making response to
requests faster and more
efficient.

The LSI-11 and its Dual Drive Floppy Disc are used to store

personal patient information, keep track of all patient requests, set priorities, locate nurses and aides, and generate hard copy reports of all system operations.

The reason Sylvania chose the LSI-11 was simple — they had to get to market fast. According to Project Manager Bill McClellan, "The LSI-11 saved us all the time it would have taken to design our own micro from chips. And to top it off, we got a nationwide service and spare parts network thrown into the bargain."

Since System Twenty-One had to be extremely easy to use, with the computer doing most of the work, software development was also an important issue.



Bill McClellan, Project Manager at GTE Sylvania, Waltham, MA.

Bill McClellan comments:
"Thanks to the LSI-11's RT-11
operating system, we were able
to do most application software
in FORTRAN, instead of the
assembly-level language other
micros require. This made for
faster, easier programming and
far simpler debugging."

In addition, "When it came to interfacing the new computerized system to our existing Nurse Call equipment, the LSI-11's optional Serial I-O card made the job a snap."

To sum up, Bill McClellan told us: "The LSI-11 gave us the size and price of a micro, with the power, the software, and the backup of a full-blown OEM mini."

The customer is always right. For 600 pages of solid technical information, plus our new brochure of microcomputer case histories, "Why Anything Less than the LSI-11 Wasn't Enough for Me," just call toll free 800-225-9220 (in Mass. 617-481-7400, ext. 5144), or write Digital Equipment Corporation, One Iron Way, Marlborough, MA 01752.

digital COMPONENTS GROUP

ficient operation in a mixed environment of both online, transaction-oriented network management and batch-oriented multiprogramming applications. Compact logic circuits, modular power supply, and high density memory are incorporated to provide powerful systems that require one-third the floor space of earlier models, and use less power.

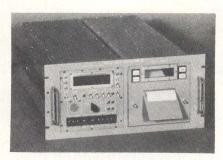
Burroughs Corp, Detroit, MI 48232 incorporated in both systems an I/o subsystem which offers up to 24 channels. Each channel has its own Data Link™ processor, which accepts I/o commands and executes them independently of the central processor, thus providing the ability to control large numbers of I/o channels with only a minimum burden on the central system. This enables the systems to handle large data bases and quantities of terminal devices simultaneously with batch processing operations.

The systems are object-code compatible with large B 3800 and 4800 systems as well as earlier systems, providing protection for user-program investments. System software includes the Master Control Program (MCP), which allocates and controls the system's total resources; Network Definition Language (NDL) for simplified data communications network design; and Data Management Systems (DMS), which relieve the application programmer of having to deal with storage and retrieval of data.

A basic B 2810 has a CPU which operates at 2 MHz and includes 125k bytes of error-correcting Mos memory (expandable to 500k bytes) with 667-ns access time. Its 8-channel 1/0 subsystem (expandable to 24 channels) transfers data at up to 3M bytes/s. CPU in the B 2815 operates at 3 MHz. Both are available in dual processor configurations, and can operate in dual processors in the 700 or 800 series. Circle 143 on Inquiry Card

Bit Error Rate Monitor Measures and Records Link Performance

A bit error rate monitor developed at the Naval Ocean Systems Center, San Diego, CA 92152 provides continuous online monitoring of link performance in the Navy Satellite Fleet Broadcast System. A general-purpose bit and



BERM II, developed at Naval Ocean Systems Center to monitor link performance of satellite fleet broadcast systems, uses p/ROMs to allow access to "canned messages" and permit observation of bit and character errors on LED display or directly from integral printer

block/character error recorder, BERM II is a second generation unit which remains compatible with existing BERM I units, but provides expanded coding capabilities.

BERM I units incorporate a variety of rates, sample sizes, and interface functions; however, they are limited to a single code, which is transmitted and compared against a reference code generated at the receive location, yielding a bit error count. BERM II fulfills these same functions and provides a variety of other features which enhance digital link performance measurements.

Consisting of an electronics module and a high speed printer module, the single unit is suitable for mounting on a shelf or standard RETMA rack. Incorporated are a LED display, directly readable paper printout, and an output for a high speed tape perforator. The LED display presents either bit or block errors. The printer records time of day, selected input channel, sample size, bit errors, user identification, receive rate, block size, block errors, flag symbol, and other selected data. All printout information can be output to a high speed tape punch. Five codes with corresponding complements ranging from 15 to 2800 bits in length are provided.

Internal programmed ROMS provide capability to access an ASCII or Baudot "canned" message. Message format plus station identification (switch-selectable) may be preprogrammed. This permits measurement and recording of link performance through observation of bit and character errors and/or the program teleprinter printout. A balanced sequence code can be accessed and results printed out for system bias measurements.

In addition to recording normal bit and block error data indexed with real time, the unit will accept 12 BCD inputs from auxiliary equipment, such as s-D converters or digital voltmeters. This permits key test parameters (eg, vessel location, receiver AGC values) to be simultaneously included in the recordings.

Switch-selectable TTL, RS-232, MIL ±6 Vdc, and 60/20-mA current loop interfaces are incorporated. Duplex operation is provided for standard data rates from 75 to 9600 baud. Superior receive bit tracking capability allows the unit to maintain synchronization during prolonged signal fading.

Built-in test equipment and test modes for unit validation and malfunction isolation permit a close to 100% integrity check of the entire monitoring system. An internal transmit code generator can be internally or externally keyed and clocked. Receive electronics can be gated by a receive modem and/or be turned on or off by built-in sensing electronics, permitting a maximum rate of data collection when the link is active and a standby mode when the link is inactive. In addition to allowing simulation or testing at the data set 1/0 ports, this capability permits operators to use operational lulls for link quality tests.

Circle 144 on Inquiry Card

Portable Digital Tester Identifies Malfunctions To Simplify Service

The 851 digital tester is a lightweight, portable, yet versatile tool that allows first line service technicians to concentrate on the problem. In the unit, Tektronix, Inc, PO Box 500, Beaverton, OR 97077 has combined the functions of a DMM, a counter, pulse width discriminators, and logic state indicators on each of three channels, to aid the technician in identifying malfunctions. The technician attaches the general-purpose probes, selects a measurement function, and reads the results directly from an autoranged digital display.

When used with documented service procedures, the 851 is an effective tool for making a variety of measurements—from checking line voltage to counting transitions of a signal be-

Now Norden gives the PDP-11/34M a little brother: the LSI-11M.



New militarized microcomputer uses same software as commercial LSI-11.



The LSI-11 M is a fullscale, 16-bit microcomputer and the smallest computer in the PDP-11 M line. Part of a newfamily of

fully-militarized computers, it uses exactly the same software as the commercial LSI-11.

Combining Norden's experience in military electronics with DIGITAL architecture and DIGITAL software, the LSI-11M offers exceptional price/performance. This is a direct result of a rich repertoire of over 400 instructions and a low hardware cost.

Familiar features plus militarized peripherals.

Available without chassis, the LSI-11M comes as a 6 x 8.2 x 1" CPU module. This module is available with 4K words of resident semiconductor memory. Further memory options in the form of 4K PROM and 16K and 32K core modules are offered. Peripheral and I/O connections are accomplished thru fully militarized serial and parallel I/O modules. The LSI-11M also has a real-time operating system (RT-11). For more information, call or write Director of Marketing, Computer Products Center, Norden Division, United Technologies Corporation, Norwalk, Connecticut 06856; Telephone (800) 243-5840 toll-free, or call (203) 838-4471.

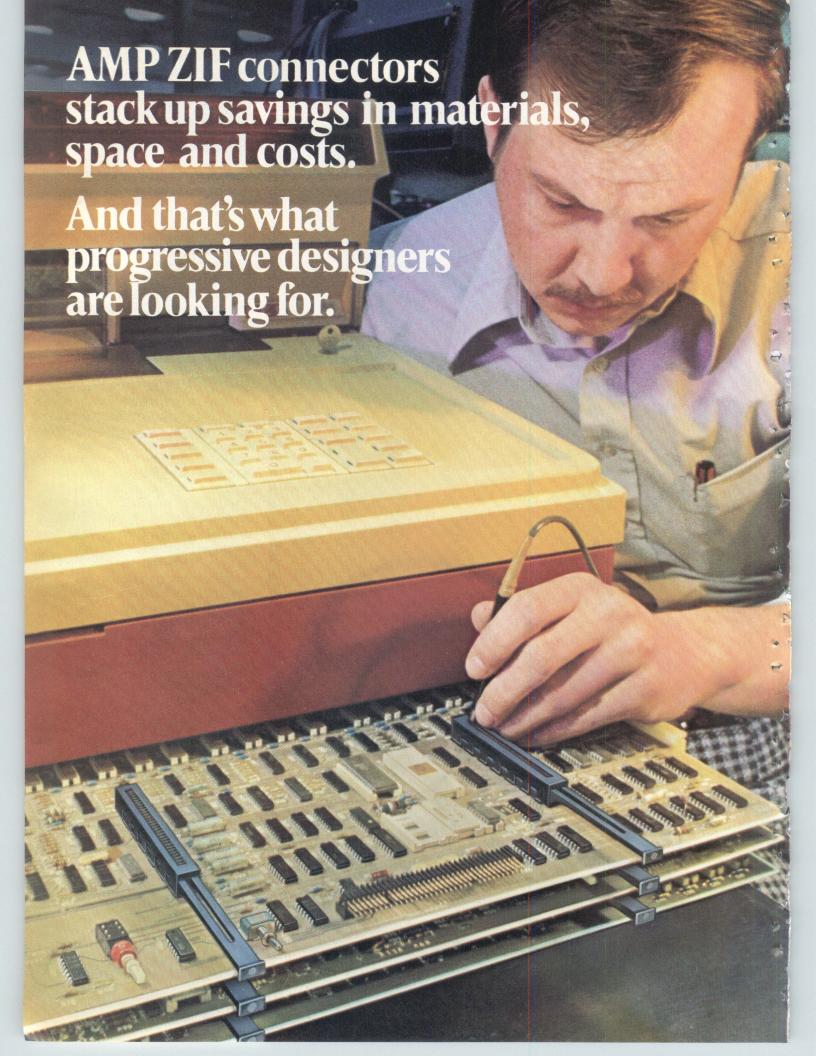
PDP-11 and LSI-11 are licensed trademarks of Digital Equipment Corporation.

PDP data processing with Norden military muscle.

NORDEN

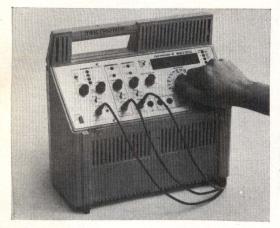


CIRCLE 26 ON INQUIRY CARD





DIGITAL TECHNOLOGY REVIEW

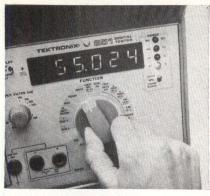


Combining functions of DMM, counter, pulse width discriminators, and logic state indicators on three channels in portable, simple to use unit, Tektronix 851 allows service technician to concentrate on problem to be solved

tween two defined events. The unit's autoranging 5-digit multimeter with floating input measures ac and do voltage and resistance. Input signal polarity is automatically checked and displayed on the DMM. Measurements are displayed directly in five decimal digits with a sign and floating decimal point. Range indicators show the order of magnitude of the display. A built-in 35-MHz counter allows gated events, transition counts, duty factors, and frequency ratios to be analyzed.

The three input channels are provided with a variable pulse-width discriminator. Input filter control can be set within a range of 50 to 300 ns; pulses below the minimum will be rejected. Logic state indicators on each channel reveal signal activity and invalid levels.

Dual-threshold input of channel A reacts only to signal levels at or exceeding upper and lower limits, which are fixed TTL levels or varied with the -30 to 30 V range. Single input



Measurement display functions of portable 851 digital tester are selected using single multiposition switch. Colorcoded bands around its periphery distinguish functions involving three channels and identify them with related threshold setting functions

threshold controls are provided on channels B and C. Indicator lights inform the operator when signals are above or below the set levels.

Measurement display functions are controlled with a single multiposition function switch. Color-coded bands around the outside of the switch identify functions that involve channel A, B, or C. Threshold setting functions are color-coded to identify the applicable channel.

Circle 145 on Inquiry Card

Medium-Scale Computer Systems Aimed At Multiuser Requirements

Systems 115, 125, and 135, slanted toward high performance, multiuser requirements, incorporate technological hardware extensions of the Series 100. Introduced by Harris Corp, Computer Systems Div, 1200 Gateway Dr, Fort Lauderdale, FL 33309, the medium-scale systems feature a single-board microprogrammed cru, Mosmemory with error correction, increased 1/0 bandwidth, multiplexing DMA channels, and communications processor.

Systems 115, designed for distributed processing applications that require multiuser concurrency, can satisfy the mixed processing needs of up to eight (local or remote) terminal users, while simultaneously communicating with a large remote system. A basic system includes 144k bytes of mos memory, 750k bytes of virtual memory, system CRT, magnetic tape unit, 10.8M-byte disc, CPU, and com-

munications multiplexer. It can handle tasks ranging from data base transactions to scientific research.

Serving commercial and scientific applications, the 125 includes 144k bytes of Mos memory, expandable to 624k bytes. With 3M bytes of virtual memory under the Vulcan operating system, the system is capable of supporting up to 32 terminal users, while concurrently performing multibatch and remote job entry operations.

Largest and most powerful family member, the System 135 has more than 12M bytes of virtual memory, and can support large data bases and more than 50 terminal users. Main memory is expandable from 384k to 768k bytes. A basic configuration incorporates 40M-byte disc with 1.2M-byte/s transfer rate, communications processor, system CRT, and magnetic tape unit.

All systems include the Vulcan operating system with seven language processors. Vulcan can concurrently support timesharing, multistream batch, remote job entry, and realtime operations. Circle 146 on Inquiry Card

Militarized Eclipse Computers Under Development

Plans to include Data General's Eclipse® computers in their military product line have been announced by Rolm Corp, Mil-Spec Computer Div, 4900 Old Ironsides Dr, Santa Clara, CA 95050. Initial deliveries will occur in 1978.

Software to be offered with the computers will include the top of the line Eclipse data base management system and the advanced operating system. To further support sophisticated applications, a line of militarized peripheral devices will be made available.

Circle 147 on Inquiry Card

Color and smarts don't cost a lot anymore.

Ramtek's new
MICROGRAPHIC™ terminal
gives you color,
intelligence, graphics,
and alphanumerics
at a price
you can afford.



Here's great resolution and a bright, flicker-free display on a matrix of 512 elements by 256 lines in a terminal that's easy to program to your requirements.

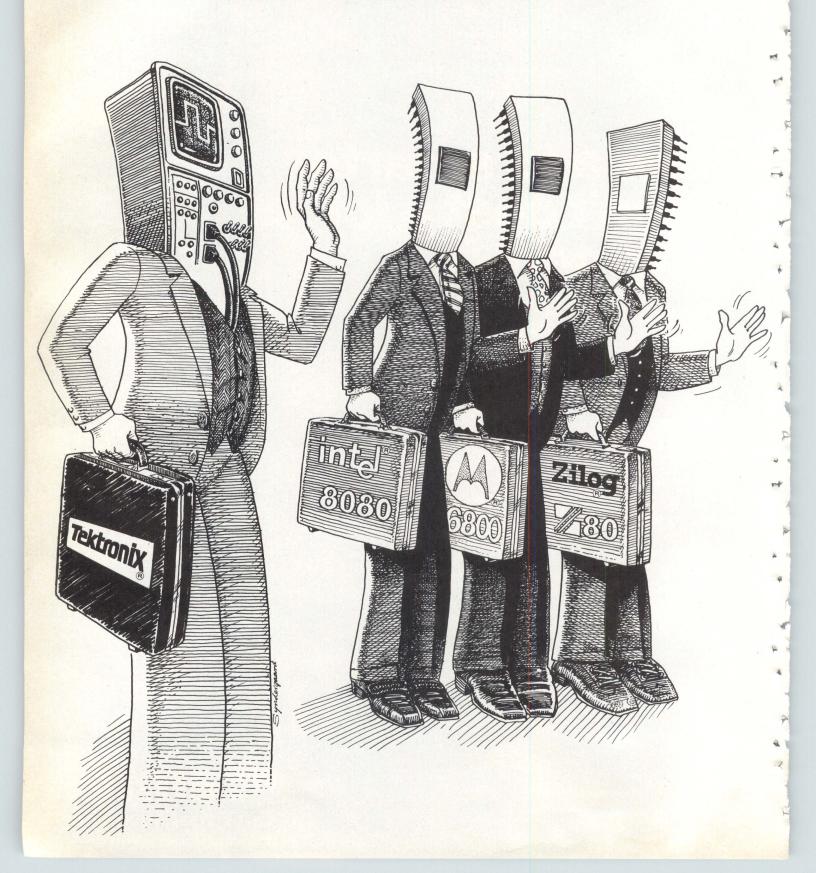
No longer do you have to put up with poor resolution in economypriced terminals. Ramtek gives you a combination of true graphics—such as vectors, conics, plots and bar charts and high-speed alphanumerics with a high-resolution industrial-quality monitor. You can choose two sets of 8 colors for both graphics and alphanumerics. Dual and split screen capability too, with all the price/performance benefits of raster scan technology. And the independent alphanumeric refresh offers you singlecharacter addressability within a visible matrix of 25 rows of 80 characters that are bright, crisp, sharp, and well defined. The refresh memory also allows selective erase, modification, and update.

The MICROGRAPHIC terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM. Ramtek's control software gives you TTY compatibility and high-level graphic functions commanded by ASCII text strings. Choose from an extensive list of options such as additional serial I/O ports, alphanumeric overlays, programmable fonts, and packaged software.

Best of all, you'll find Ramtek gives you an affordable price, depending upon your individual requirements. Find out more by contacting us. We're Ramtek, 585 N. Mary Avenue, Sunnyvale CA 94086. In a hurry? Pick up the phone and call us at (408) 735-8400. We'll tell you why you can afford color and smarts.



Are you rushing into microprocessor-based development with old friends?



You have a new friend.

You don't have to pay a big name price for a universal product development lab. And, don't let your fondness for a certain chip lead you to a convenient but confining marriage. The inevitable divorce will be costly and time consuming. If you want to develop products happily hereafter, move in with Futuredata.

Futuredata systems are universal.

We can move you into multiple-microprocessor-based product development at half the cost. With the largest selection of powerful hardware, software and economical peripherals around. With high speed disk or low cost tape operating systems. With incircuit emulators for 8080, 6800, and Z-80. With the universal microcomputer that tackles every job.



Only Futuredata can move you in for \$3850.*

No other microcomputer can match the cost/performance standards set by our MICRO-SYSTEM/20 & 30 disk-based systems and our MICROSYS-TEM/10 & 15 tape-based systems. Each of these are complete development systems with up to 56K memory, 960 character CRT, ASCII keyboard, two RS-232 * serial ports, 8-bit parallel I/O, realtime clock, bootstrap in PROM, 8level vectored interrupts and complete disk and tape operating systems with monitor, debugger, editor, assembler and utility.

*Domestic U.S.A. prices



The most complete spectrum of economical systems.

Move in with our Dual 5" Mini Floppy Disk System, our Dual 8" Standard Floppy Disk System, our unique QUICKRUN™ 32K Tape Operating System or our new Universal Dual Development System. No matter which you choose, the savings will be significant.

Only Futuredata has QUICKRUN™

MICROSYSTEM/15 has the only co-resident assembly and interactive debugging system in the industry. With editor, assembler and debugger/monitor all in memory, things happen fast. Assembly of a 1000 statement program takes a mere 15 seconds. At \$5275,* it's the most cost-effective development tool around.

Now the first Universal Dual Development System.

Futuredata has combined two separate memory / processor sys-

tems in one host computer. Mix or match processors, disk or tape operating systems in each half. Put two development engineers to work at full speed, simultaneously. You get two complete systems in one and save nearly \$2000.



In-circuit emulation and higher-level language.

We have in-circuit MICROEMU-LATORS™ for 8080, 6800, Z-80, Extended BASIC, line printers, EPROM programmers, hardware, software, documentation and a rock-solid record for reliability. So, let's be friends!



30-day "Get Acquainted" offer.

Try one of our development systems for 30 days at no risk. For more information, write or call Futuredata today.

Move into product development with a new friend...

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Add-On Memory System Increases 370/158 Main Store to 16M Bytes

An add-on memory system, STOR/158-4, increases main storage capacity of IBM System/370 model 158 computers to 16M bytes. The memory, implemented by Cambridge Memories, Inc, 12 Crosby Dr, Bedford, MA 01730, permits attachment of 16M bytes of storage to uniprocessor, multiprocessor, or attached processor versions of 158 model 1 or 3; this compares with IBM limits of 4M and 6M bytes for uniprocessor models 1 and 3, respectively, and 8M and 12M bytes for multiprocessors 1 and 3.

According to the project engineer, Steve Schwartz, implementation of the system required simple extension of the memory address field. "The address bits have been there all along." Schwartz also pointed out that IBM provides store protection, which prevents unauthorized access to programs within multiprogramming systems up to a limit of 8M bytes. "To accommodate our expanded system, we designed a store protect card employing ECL random-access memory devices."

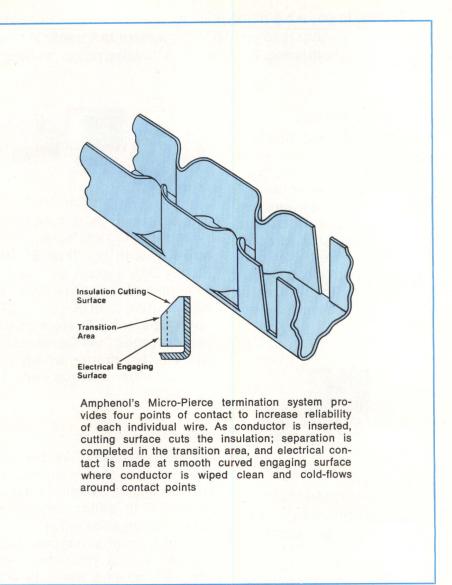
Circle 148 on Inquiry Card

Solderless Connector Speeds Cable Assembly in Field or Factory

Cables can be terminated in the field to exact length without danger of solder splash or bridging using the 157 series Micro-PierceTM termination system introduced by Amphenol North America Div, Bunker Ramo Corp, 900 Commerce Dr, Oak Brook, IL 60521. Terminating a 25-pair cable requires less than four minutes using a specially designed field termination tool. An additional advantage is that terminated wires can be easily removed and replaced.

Heart of the connector system is a terminal that provides a full four points of contact. Each electrical contact consists of insulation cutting surface, transition area, and electrical engaging surface. Electrical contact during termination is made in a 3-step process.

As the conductor is inserted, the cutting surface of the terminal cuts or shears the insulation; then, in the



transition area, the insulation separation is completed. Host electrical contact is made at the smooth, curved engaging surface. As the bare wire reaches the bottom of the engaging area it is wiped clean and actually cold flows around the contact points.

The wire is compressed with a force of about 3 kg to a depth of approximately 0.002" x 0.0095" (0.05 x 0.24 cm) wide to conform to the size and shape of the engaging surface. The result is a relatively large, gas tight contact area that is free of corrosion and foreign material for maximum electrical flow with low resistance. While the conductor is compressed into the terminal, the force acting on the ductile wire is not great enough to nick or cut it; this eliminates stress points that would be susceptible to

damage from vibration or handling. A strain relief built into a lock wire channel in the dielectric holds and supports each individual conductor, and removes the point of stress from the terminal area so that it is unaffected by physical movement.

Connectors are offered in 14-, 24-, 36-, 50-, and 64-contact configurations, and in rack and panel, cable to panel, and cable to cable mounting styles. Design features include a glassfilled volax dielectric that is capable of withstanding continuous temperatures to 275°F (135°C) and cadmium copper contacts with 30 µin (0.762 µm) gold over copper flash plating. Connectors are completely intermountable and intermateable with solder equivalents to facilitate retrofits.

Circle 149 on Inquiry Card

NOW DELIVERING

The 1602A A lot more computer in a smaller package

We've taken our proven and powerful 1602 (AN/UYK-19) and doubled the internal memory to 64K, developed a single microprogrammed CPU module, included space for seven I/O interface boards and two RAM/ROM slots, and value-engineered the whole package into a single 191/2 inch ATR chassis. In the process we trimmed off weight and added a combined Floating Point/Built-in

End result—You get a microprogrammed military processor with a 150 to 250 nanosecond microcycle time that's most economical in terms of size, weight and memory requirements. And it's absolutely compatible with your previously developed 1602 software.

What we didn't reduce is our extensive set of software, our quick delivery and our world-wide service.

Test (BITE) capability . . .



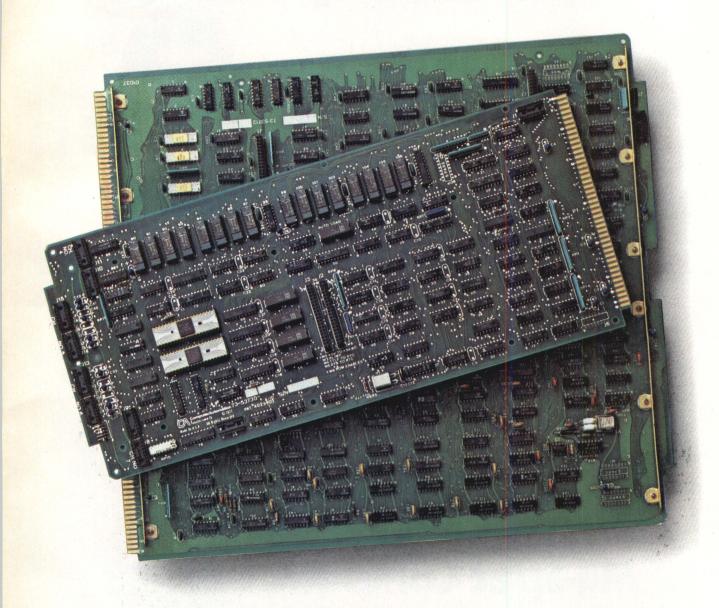
That's Why We're #1 in Mil-Spec Computer Systems



MIL-SPEC Computers

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BRAND NEW MINICOMPUTERS



BRAND NEW BROCHURE



Circle Reader Response No. 115



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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Program Flexibility of Microprocessor-Controlled Elevators Enables Easy System Modifications

How many passengers do elevators carry annually in the United States? 40 billion? 50 billion? 60 billion? One source says 54 billion; but since there is no way to count all elevator riders, that number can only be an estimate—even if based on careful studies. In any event, the number is huge—considered on a world-wide basis it becomes astronomical.

However, despite the large number of elevators in the U.S., control systems for elevator banks or even individual elevators are not mass produced. Control requirements are so diverse that there can be no uniformity. Speeds vary from as low as 25 to more than 1200 ft/min (7.6 to 365 m/min). Lifting capability varies from a few hundred pounds to several tons. Even duty cycles differ: they range from only occasional to nearly continuous operation. In addition, the number of floors served, locations and types of entrances, and indicator patterns differ widely among various installations. Safety ordinances and standards vary, too, depending on state and local building codes.

Some commonality does exist in basic elevator motor and door control units. Yet, most other control subsystems have historically been custom designed and implemented with hardwired logic and electromechanical relays. Large high rise elevator installations have required hundreds of relays housed in several large cabinets (Fig 1), with resultant, inherent problems of maintenance.

One evident solution to this problem has been digital computer control, but that sometimes resulted in added

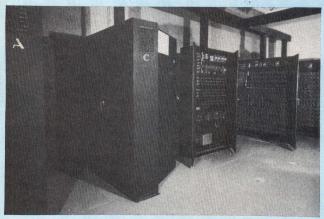


Fig 1 Photo of hardwired control system cabinets for large elevator installation. Hundreds of electromechanical relays are required

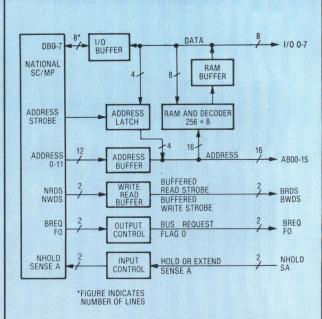


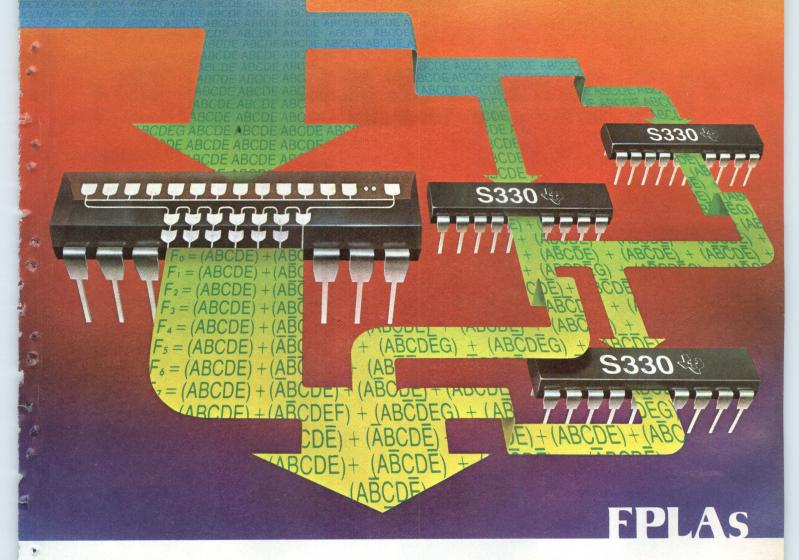
Fig 2 Diagram of CPU board in Montgomery Elevator Co control system. National Semiconductor SC/MP microprocessor serves as central controller with 256 words of scratchpad RAM

cost and did not always save appreciable space. Since 1973, however, Montgomery Elevator Co of Moline, Ill has been designing elevator control systems using microprocessors.

Originally this elevator manufacturer used Intel 4004 microprocessors in four field-test installations. Later, it adopted 8-bit SC/MP microprocessors from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Fundamental Control Configuration

Internally, SC/MP is a programmable 8-bit parallel processor implemented on a single IC chip. It contains one 8-bit accumulator, four 16-bit pointer registers (one of which is dedicated as the program counter), an 8-bit status register, and an 8-bit extension register. Up to 4k bytes of memory can be accessed with its 12-bit latched address bus output, and four extra address bits are multiplexed and sent out on the data bus with the address-ready strobe to attain full 16-bit addressing.



New dimensions in logic...

Field Programmable Logic Arrays. From Texas Instruments.

TI's new S330 and S331 Schottky TTL FPLAs open new dimensions in logic design. They feature a unique built-in capability for multidimensional expansion of the basic 12 input x 50 term x 6 output organization. A flexible means for achieving more efficient designs.

Automatic enable

A special circuit resides dormant in TI's new FPLAs. Fuse a single link and the FPLA turns "smart". Automatically enabling itself by decoding true product terms. Result: Multidimensional expansion to almost any size array. You expand variables, product terms, and outputs. Without external components, logic or control.

Efficient, flexible, user programmable

Use these LSI FPLAs to replace standard SSI and MSI logic functions. To implement unique random logic. To supplement PROMs.

They're field programmable. Using proven titanium-tungsten fuse links for fast, low-voltage, reliable programming. You can "wire up" whatever combination of AND, NAND, OR, NOR logic that most precisely fits your design. Reducing design time. Package count. And cost.

20-pin Schottky TTL

With the S330 and S331, you get the high performance of TI's

Schottky TTL. Typical delay time: 35ns. Typical enable time: 20ns.

They come in TI's space-saving 20-pin plastic or ceramic packages. For greater board density, greater reliability, lower cost. In both commercial and military applications.

Useful, economical

The SN54S/74S330 (3-state output) and SN54S/74S331 (2500-ohm passive pullup output) are both available now at \$9.00 for commercial (plastic) versions (100 pieces).

Order today from your TI distributor. Or for more details, write Texas Instruments Incorporated, P.O. Box 5012, M/S 308, Dallas, Texas 75222.



TEXAS INSTRUMENTS

INCORPORATED

THE GUTS OF A WINNER:



Not just the first 24 MB disk drive —but every inch a champion.

Leading the field in the stretch to 24 MB disk storage: Pertec's D3400 Series. The first cartridge disk drives to double traditional 3-12 MB capacities... without handicapping OEMs.

Meaning: we're not about to boost your data payload by burdening you with expensive penalties—in hard currency, or harder work. Like controller redesign. Like interface snafu's. Like requiring special pre-recorded media. No way.

Familiar technology. D3400 drives fit neatly into Pertec's most advanced disk product line, D3000—as members of a fast-access family you've been living with right along. And completely interface compatible with standard industry configurations. Ours *and* other manufacturers.

One unit: four platters. Available in front or top load models, D3400 expands to 24 MB through 3 fixed and 1 standard media-interchangeable cartridges. All with independent write protection.

Easy installation and maintenance. This 24 MB disk drive looks just like any 3-12 MB unit: same size, same rack space. And the same exclusive Pertec hinge-mounting of PCBAs—simplifies access to the electronics, reducing oper-

ational and service costs.

Champs in reliability. Each D3400 cartridge disk drive has to meet the same tough criteria—in production and on-line—that protects every Pertec product, and every OEM investment.

In short, we're producing a bigger storage appetite, but assuring you the same pre-tested, high performance, field-proven drives that have made Pertec the odds-on favorite with OEMs for years.

No-compromise service. One out of five people in Pertec Computer Corporation is a full-time contributor to the most comprehensive OEM-support organization in the field today.

Sales service that expands and cost-optimizes your configuration options: we'll help you target in on the D3000 system that precisely meets your specs—pick from 3 MB to 24 MB on cartridge disk. And the same support goes for our fixed and flexible disk drives—just ask.

Field service facilities are strategically located throughout the world. Trouble-shooting is as close as our toll-free 800 line—open for business around the clock.

And it's that kind of commitment that ranks us today as the world's largest independent manufacturer of peripheral equipment.

Cartridge Type	Capacity (Megabytes)	Platter Configu- ration	Bit Density (bpi)	Speed (rpm)	Model Number	Quantity Required	Date Wanted	Send Specs Only
5440				1500	D3461			
Top Load 24.0 QUAD	QUAD	2200	2400	D3462				
2315			7 10	1500	D3481			
Front Load	24.0	QUAD	2200	2400	D3482			
Name					/			
Title			Phone			Ext		
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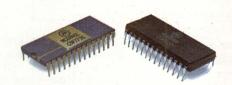
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The MC6840 programmable timer is designed for applications requiring frequency measurement, event counting, interval measurement, square-wave generation, gated-delay signals, single pulses of controlled length and pulse-width modulation . . . to name just a few.

Three 16-bit binary counters with the corresponding control registers and a status register are utilized on the chip. The counters are under software control and can be used to cause system interrupt and/or to generate output signals. After interrupts, counting restarts to allow determination of time

since interrupt. Control bits enable interrupts, outputs, counter configuration and control capability.



Both plastic and ceramic 28pin 6840 packaging is available now for the 1.0 MHz version of the device. Higher speeds up to 2.0 MHz are scheduled for availability in the near future.

As with all M6800 family parts, the MC6840 benefits from the complete software, hardware, and bus compatibility of the family.

Introduction of the original M6800 Family back in the early days of microprocessors took a major commitment. Based on independent and user reactions, the results were well worth the effort. But important as they were in pioneering a new direction for the microprocessor, the compatible family concept, that commitment and those results are dwarfed by our present program.



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	Control Register 3
100	
Ĺ	Control Data Bus
	Desistan C Interface
	Register 2
-	Control Register 1 Segister Register Segister Se
4	
7	
	Latches Counters Counters Counters
	Counters Counters See MSB See Counters
	Latches Counters
	Counters Counters LSB MSB
	S o Latches Latches × in
	Counters Counters
	LSB MSB
8	
*	LSB Buffer Status Register Register
N N	LSB Buffer Status

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Architecture includes on-chip oscillator and timing generator, latched 12-bit Tri-state address bus, 8-bit Tri-state data/control bus, and two serial I/O ports. The microprocessor also has three program-controlled output flags and two program-tested sense inputs for single line peripheral control. On-chip functional capabilities reduce the number of necessary support circuits and simplify system design. In addition, the device is adaptable to multiprocessing.

Overall gain from microprocessor-based logic control over electromechanical-relay control has been significantly reduced engineering and manufacturing costs, improved reliability, and lower maintenance requirements. Only 12 basic circuit boards are required: one CPU, one p/ROM, one I/O interface, one timer, one power supply, one input, and three output driver boards, plus three motherboards. With these boards the Montgomery microprocessor elevator control system can accommodate all elevator types—from relatively simple, hydraulic freight units to fast, complex multicar passenger installations.

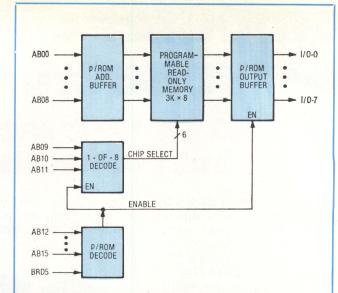


Fig 3 Diagram of p/ROM board, one of 12 boards in typical elevator control system. In addition to 12 buffered address lines, four data lines are decoded to give 16-bit address capability for page-reference memory and peripheral addressing

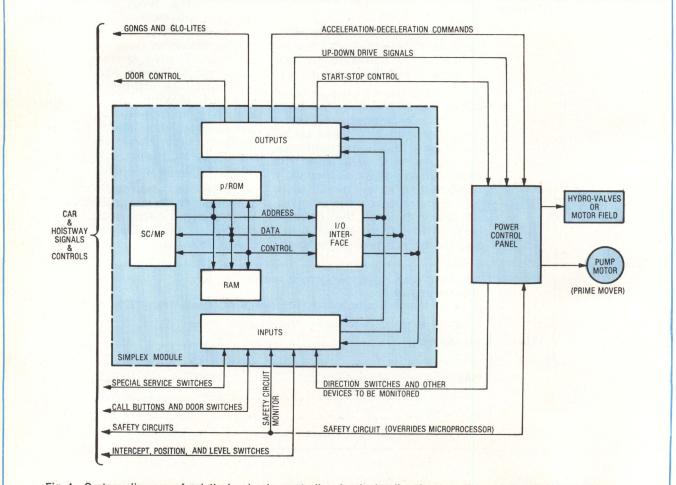


Fig 4 System diagram of relatively simple controller for hydraulic elevator. For safety, electrical and mechanical interlocks inhibit elevator operation

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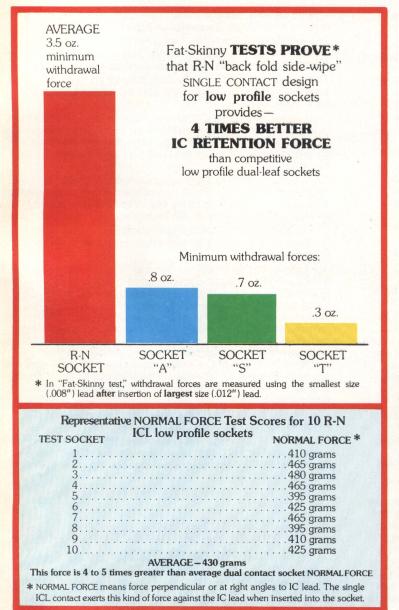
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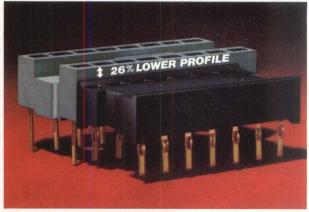


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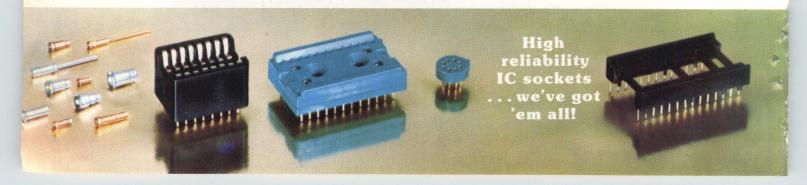
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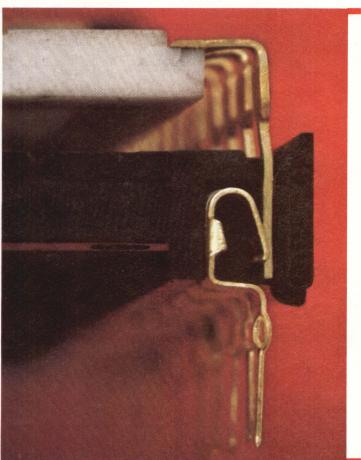


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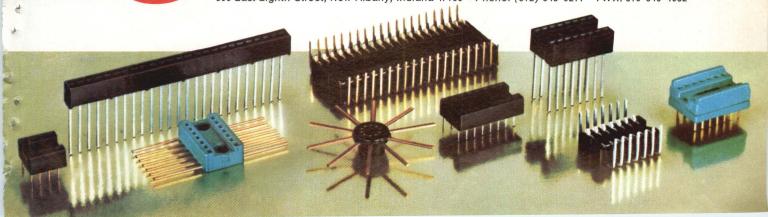
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DIGITAL CONTROL AND AUTOMATION SYSTEMS

The CPU board (Fig 2) consists basically of the microprocessor and 256 bytes of random-access memory (RAM) organized 256 x 8 as scratchpad. Four address bits on the data bus are latched and used as additional address lines to select memory pages. Standard 12-bit address lines specify discrete memory locations within the page. All 16 address lines are decoded even though the full 16-bit memory-address capability of the microprocessor is not needed on small elevator systems. This allows production of similar boards for both small and large installations and, in addition, aids test tool programs which occupy separate memory pages.

The p/ROM board (Fig 3) contains socket positions for up to 3k x 8 bits of programmable read-only memory. Its configuration enables use of a fully populated board on large installations and less dense versions for smaller systems; again similar boards are built for all systems, saving production costs.

Circuitry of the input board senses switch closures and relays the information to the CPU board; the microprocessor sends commands to the switches as 48-Vdc and 117-Vac control signals from the output boards. All input, output, and 1/0 interface boards are designed to prevent any erroneous commands caused by the emission of spurious signals common to the high electrical noise environment of heavy machinery applications.

Functioning at 14 V, cmos circuits provide wide logic thresholds. Input lines are optically isolated and filtered. Radio frequency interference is held to an absolute minimum.

Small System Control

Basic configuration for control of a small hydraulic elevator (Fig 4) consists of a Simplex module comprising CPU, memory, power supply, and I/O boards. Instead of the banks of electromechanical relays of one of the cabinets in Fig 1, this relatively simple controller is housed in a small, wall-mounted unit such as (with cover removed) in Fig 5.

Input cards, initially, sense standard safety-interlock circuits such as hoistway and elevator car door positions. When interlock signals are in the correct sense, the elevator responds to appropriate hall or elevator call buttons, initiating car coming and car position lamps. If, for example, the car is below the called floor, the microprocessor initiates pump motor contactors. To allow the motor to start under minimal load, the microprocessor provides the timing necessary to allow motor startup prior to actuating the up-valve solenoid. The elevator proceeds upward until hoistway sensors signal the microprocessor to decelerate and stop the car at the selected floor.

In downward direction the motor is not used. The microprocessor opens a pilot solenoid valve, allowing the hydraulic fluid to return to a reservoir. When hoistway sensors indicate the car is approaching the selected floor, the main valve is modulated to decelerate the car for the final approach and closed to stop the elevator at the desired position.

Large System Control

Simplex modules are also used for large, multielevator installations (Fig 6). However, individual modules are supplied for each elevator, for the master control, and for system diagnostics.

Each module operates independently, sensing critical parameters for its elevator, such as conditions of safety interlocks and car call buttons as well as car position in the hoistway. Signals from the modules are provided to a power controller to enable operation of drive motors, doors, lighting, and car position and hall indicators.

For overall control, the modules are multiplexed on a rotating priority basis with a master or common micro-

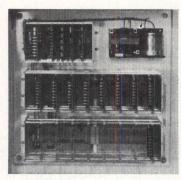


Fig 5 SC/MP-based controller for hydraulic elevator. Compare this small, compact, wall-mounted unit to one of electromechanical relay cabinets in Fig 1

processor, again a SC/MP. Modules transmit car cable, elevator travel direction, and hoistway position data to the master controller which uses all such information in making its decisions. In addition, data common to the overall system are collected by the master controller and assigned to relevant modules.

This master controller also supplies overall system logic, using the same 12 basic cards that make up each Simplex module. Hall calls are sensed by input boards, and output boards supply call indication. The CPU board includes the 256 bytes of RAM, but additional workspace RAM can be added in 3k increments. System logic is partitioned in 1.5k to 3k of p/ROM. These subroutines also provide elevator operation scheduling.

An example of the sophisticated control that has been relegated to these microprocessors is the variation of decisions based on operating procedures for different times of day. Typically, at night or on weekends or holidays when there is little passenger traffic, elevators function in demand mode. Elevator cars are shut down in varied locations to provide balanced service. When a hall call occurs, the master controller initiates the car nearest to the floor requesting service. When the passenger has been delivered to the selected floor, the system redistributes cars throughout the hoistway.

In the morning rush period, passenger traffic is predominantly upward. Therefore, the controller initially positions all cars at garage or lobby floors. Then, as each car reaches the highest floor designated by its passengers, the controller reverses that car's direction and

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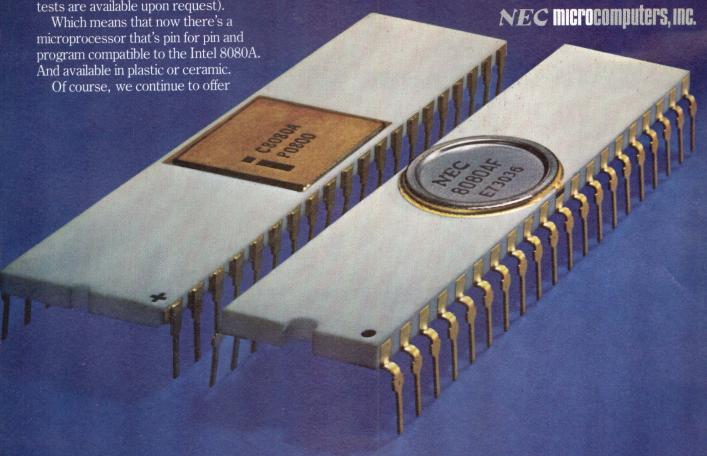
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For technical data, circle 35 on Inquiry Card. For a demonstration, circle 36 on Inquiry Card.

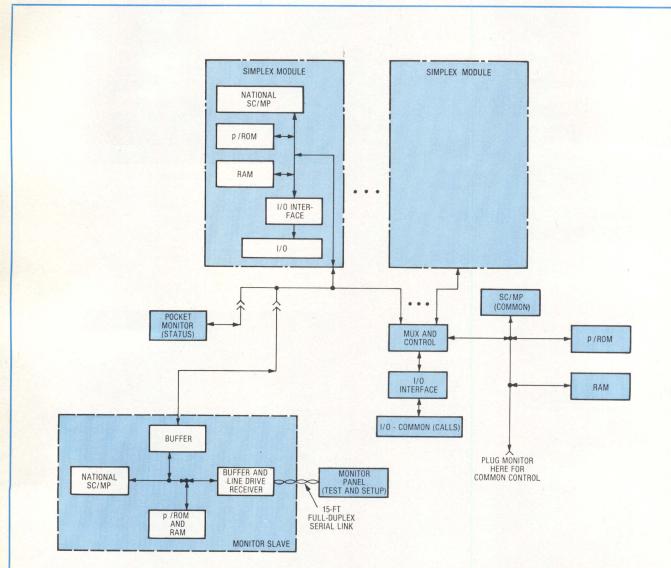


Fig 6 System diagram for multi-elevator control system. Up to eight Simplex modules control individual elevators while master controller provides overall system control. Pocket monitor gives check of Simplex module status. Monitor panel slave uses microprocessor to form intelligent diagnostic tool

returns it to the main floor, routinely picking up downtraveling passengers. However, the master controller notes down calls from upper floors and orders the elevator with the highest car call to continue upward to pick up the passenger before reversing.

When the initial upward traffic pattern ebbs, the system is placed into a mode that allows interfloor passenger travel. The master controller, for example, might place one car at the main floor and one at the

top, and set several others to move up and down as passenger requirements dictate. When a downward traveling car reaches the main floor—or an upward traveling car arrives at the top—the car being held there is dispatched.

Another mode takes over for the evening rush—this time downward, with nearly everyone trying to leave at one time. Based on previously made passenger traffic counts, the master controller distributes elevator cars



Production economics was only one of the factors that had to be considered in the selection of material for the cabinet of the new Conrac model 480/25 CRT terminal. Design, engineering, performance and appearance considerations also figured strongly in the eventual choice of molded Baydur urethane structural foam for this demanding

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DIGITAL CONTROL AND **AUTOMATION SYSTEMS**

throughout the building just prior to the rush, with several on the most heavily populated floors. If passengers on lower floors are passed up because down elevators are fully loaded and therefore will not stop, the controller after a predetermined time may dispatch elevators specifically to pick them up.

Two troubleshooting aids were developed for service personnel (Fig 6). The first is a relatively simple lightemitting diode (LED) pocket monitor that accesses the Simplex module control, address, and data buses. The unintelligent device lets the serviceman observe elevator functions and other operations. From these indications he can quickly determine the trouble and make necessary repairs.

In addition, an extensive, intelligent system diagnostic unit that is a standalone instrument gives service personnel complete control over the elevator installation and provides board-level diagnostics through p/ROM-resident routines. This unit has a control panel that accesses a microprocessor through its internal RS-232 ports. From the machine room, the serviceman can set hall and car calls, inhibit door operation (to prevent passenger access to elevators being serviced), analyze safety interlocks, and check functional logic.

To determine p/ROM conditions, the unit performs checksum calculations and compares them with predetermined checkbits. For I/O board diagnostics the monitor stresses input circuits with 117-V signals and monitors output logic signals; conversely it applies appropriate logic to output boards, loads them, and measures the output signal level.

Programming

Basic software and firmware programming was accomplished by Montgomery on an IMP-16 prototyping system with 16k x 16 bits of RAM and a dual floppy disc drive. Purchased software includes the SC/MP/IMP-16 cross assembler, IMP-16 Debug, SC/MP Promsoft, and Kitbug. Cross assembler and Kitbug were modified to adapt the programs specifically to Montgomery requirements. A main executive program retrieval system was also added.

SC/MP software and firmware were built using topdown structured programming. Since virtually no two elevator installations are the same, the elevator executive program has a relatively small common loop which controls the specific subroutines for the job. Each modular subroutine addresses a specific function such as six different door operations, any of the various "fireman's" controls, safety circuit sensing, hall and car call functions, motor control, five different elevator service operations, car position, and drive/start functions.

ommonwealtr

Chicago's Commonwealth Edison uses Ramtek color graphic displays for rapid display and status reporting of pipelines, valves, pumps, and other generating station data. A clear, color-coded display is updated every 5.0 seconds, giving nearinstantaneous visual scan-log-alarm functions, bar graphs, one-line piping diagrams, flow status, etc.

Before the Ramtek systems were installed, status reporting was by hardwired mimic boards, black and white alphanumeric CRTs and typers.

The Ramtek system not only costs less, it also allows more information to be presented to the operator in a form that is quickly and easily under-

stood. This results in better operator efficiency, and faster alarm reaction time. In Commonwealth Edison's 16,000 Megawatt system, thirty Ramtek color graphics displays will be utilized.

Elevator control system memory is mapped for flexible addressing of I/O, with all symbols assigned according to the requirements of a specific subroutine. All routines and subroutines are stored in the IMP-16 disc library. Job specifications, such as number of floors, location of doors, types of indicators, and master control are typed into the prototyper which spells out the appropriate routines.

An IMP-16 applications program defines the I/o symbols and assigns unique bit and byte locations in memory. The subroutines are then assembled along with appropriate tables generated by the IMP-16. By using a specially designed elevator simulator that interfaces with the IMP-16 and with a teleprinter through a SC/MP, the control software can be thoroughly debugged before p/ROMs are burned.

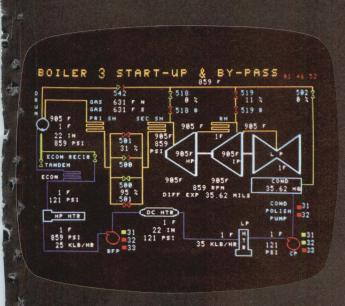
Advantages of Microprocessor Control

Although nearly all elevator control features could be handled by hardwired logic, and have been in the past, "program flexibility of microprocessor control provides significant economies when changes must be made," according to Ernie Seggebruck, Montgomery's manager of research and development. Buildings are often designed with space reserved for future extra elevators or with

capability to add floors. "In these instances, field modifications will always be faster and more economical with microprocessor control." Minor redistribution changes could be covered by reburning a p/ROM. Even major changes requiring additional controllers and the cost of on-site labor can be less expensive than required for hardwired logic.

In addition, John Bril, an electronic engineer in Montgomery's research and development, points out that since SC/MP is capable of static operation with no required refresh circuits, circuit complexity and cost are reduced in installations where elevators are idle for long periods of time. "On these installations, a simple RC circuit in conjunction with the on-chip oscillator timing generator replaces the crystal usually required with microprocessors."

Seggebruck says that "previously with relay control we had to design the controller for each job, specify all the parts, produce wiring lists, draw circuit diagrams, and then have each controller wired by hand. This was obviously a time-consuming and expensive effort. With the new microcomputer-based engineering system, we estimate up to 50% reduction in engineering time. Reduction of manufacturing time for the control system varies considerably, from 20 to 30% for a small installation up to 50% for a large one."



Commonwealth Edison monitors on-off, full-empty, flow status, and other parameters on a Ramtek FS-2400. Color is assigned for steam, water, no-flow, and oil flow to differentiate visually between materials and status. On the RM-9000, resolutions from 240 lines x 320 elements to 512 lines x 640 elements are available.

Commonwealth Edison is but one of a growing number of customers who are finding that Ramtek's raster scan modular graphics and imagery systems are giving them the expandability, flexibility, and increased productivity they need. Besides the basic alphanumeric and imaging capability, Ramtek offers a wide variety of other functions including graphics—vectors, conics, plots, bar charts—pseudocolor, and grey-scale translation.

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CIRCLE 39 ON INQUIRY CARD

DC&AS BRIEFS

Computer-Automated Factories Predicted a Reality in This Century

If a number of technological forecasts are correct, computer-automated factories will become a common reality within 10 years—rather than the novelty such facilities are at present. At the 41st Annual Westinghouse Machine Tool Forum,* M. Eugene Merchant, director of research planning for Cincinnati Milacron quoted a number of Delphi-type forecasts** made in recent years.

Out of 94 events forecast by an international panel of manufacturing research experts, carried out by the International Institution for Production Engineering Research in 1971, on which there was good consensus, 24 strongly foresaw the coming of computer-automated factories. Three of those events, according to Mr Merchant, summarize the nature and timing of that major development:

(1) By 1980 (median date) a computer software system for full automation and optimization of all steps in the manufacturing of a part will be developed and in wide use.



- (2) By 1985 (median date) full online automation and optimization of complete manufacturing plants, controlled by a central computer, will be a reality.
- (3) By 1990 (median date) more than 50% of the machine tools produced will not have a standalone use, but will be part of a versatile manufacturing system, featuring automatic part handling between stations, and being controlled from a central process computer.

Another Delphi forecast, using a panel of U.S. manufacturing personnel and carried out by the Industrial Development Div of the University of Michigan, stated that

- (1) By 1980 a computer software system for the full automation and optimization of all steps in parts manufacturing will be used for at least 25% of all parts.
- (2) By 1988 half of the total machine tools produced will be for use in versatile manufacturing systems.

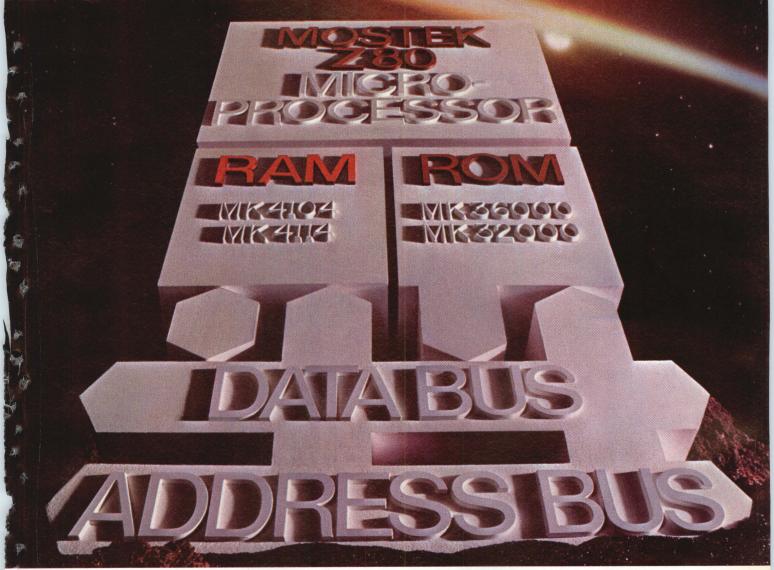
In a third procedure, carried out by the Society of Manufacturing Engineers in cooperation with the University of Michigan and the National Machine Tool Builders Association, a panel of managers and engineers from U.S. metal-working companies, forecast that

- (1) By 1985 computer software systems for automation and optimization of all steps in manufacturing planning (selection of machining sequence, selection of machine tools, clamping, selection of sequence of operations, tool selection, selection of optimum cutting conditions) will be used by at least 25% of the firms represented by the panelists.
- (2) By 1987 approximately 15% of total machine tool production will not have a standalone use, but will be part of a versatile manufacturing system, featuring automatic part handling between stations and controlled from a central process computer.

Mr Merchant stated that, while these three forecasts differ somewhat in their predicted timing for individual events, they all forecast a strong and rapid trend toward development and wide utilization of computerautomated machine tool systems, as well as the realization of computer-automated factories, based on such systems, before the end of this century. However, knowing the realities of industry, he believes that they are not really likely to happen "unless there are strong economic and social forces and incentives at work to move the world in this direction and unless there are significant R&D programs already underway generating the technology needed to make these changes." He believes that testing of the recent forecasts "of rapid development and implementation of such systems and factories lends considerable weight to their realism. Further, it should provide strong incentives to individual U.S. manufacturing companies, and in fact the entire U.S. industry-university-government complex, to actively and cooperatively pursue the rapid development and implementation of computer-automated machine tool systems and eventual computer-automated factories."

^{*}Pittsburgh, Pa, June 8 and 9, 1977.

^{**}Such forecasting uses the anonymous intuitive consensus opinion of a panel of experts as to the nature and timing of future technological events.



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DC&AS BRIEFS

Aircraft Landing/Take-Off Noise Levels Identified and Monitored by Computer Systems

Computerized noise monitoring systems installed in a number of major airports rank the severity of aircraft noise in comparison with other sounds in neighborhoods adjacent to the airport. The purpose is to provide investigators with a better understanding of the contribution jet aircraft make to total ambient noise levels in a given area. This in turn will lead to establishment of flight plans and landing procedures that reduce the level of noise disturbance in the communities surrounding the airports.

The systems, which incorporate remote microphone installations monitored by minicomputers over leased telephone lines, calculate updated noise indexes from data that are continually recorded, processed, and compared with previous data results. These indexes are used to analyze cost-effectiveness of such noise relief programs as the 2-segment landing approach, by which a landing aircraft descends from a 6-deg to a 3-deg glide slope during approach, instead of a steady 3-deg approach. Thus, the airplane flies higher and quieter over populated areas near the airport.

Designed by EG&G Hydrospace-Challenger Group of San Diego, these systems include minicomputers made by Sperry Univac Minicomputer Operations, 2722 Michelson Dr, Irvine, CA 92713 to perform four major functions: data acquisition and processing, visual and aural display, identification of exceptionally loud noises from individual aircraft, and data printout. Strings of remote monitoring subsystems are located at various sites in local communities ranging from one to five miles from the airport runways. There are 12 at Los Angeles, three at Ontario, 12 at San Diego in California as well as 17 at Honolulu, Hawaii and 10 at Dulles International near Washington, DC.

The computer is programmed to distinguish between aircraft noise and other community noise by using a tracking and screening program that takes into account such factors as sound duration, its build up and fall off, and its route from site to site. It keeps two separate noise-level tallies—one for aircraft averages and one for all others.

Noise-level averages are produced by the computer every hour for every site, and daily, weekly, and monthly totals are made (weighting evening noise higher because it is more noticeable and disturbing to community members). Individual aircraft can be identified by recordings made through the system of the actual noise picked up at a site plus the tower-to-aircraft conversations identifying the flight number. Operators may also listen to specific sites using a separate telephone line.

Circle 160 on Inquiry Card



Mostek's \$995 SDB-80 delivers Z80 power and 16K bytes of RAM.

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For OEM applications, the SDB-80 is one of the most powerful, yet low-cost microcomputers available in the industry. For \$995 (single unit cost), the SDB-80 single-board microcomputer provides Mostek's Z80 CPU (MK 3880), eight MK 4116 16K RAM memories, two PIO's (MK 3881), one CTC (MK 3882), serial ASCII interface (110-9600 baud) sockets for up to 5K bytes of PROM or 20K bytes of ROM, plus a fully-buffered and

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For software development, the SDB-80 is available with a complete package of software development aids in ROM. This optional 10K byte firmware package may be located in sockets on the board to provide the ability to generate, edit, assemble, execute, and debug programs for all types of Z80 applications.

For users requiring even greater system capability, the SDB-80 is expandable with the use of optional add-on boards. In this way, the user may configure his system to include any amount of PROM, ROM, RAM or I/O desired, plus add such features as in-circuit emulation, floppy-disk interfaces, and PROM programming capability.

For more information on the SDB-80 and the complete range of optional support boards, software, and boxes, contact your local Mostek sales office or representative.

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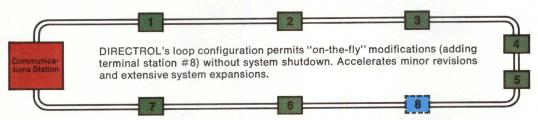
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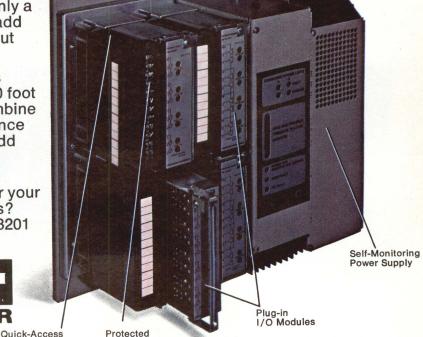
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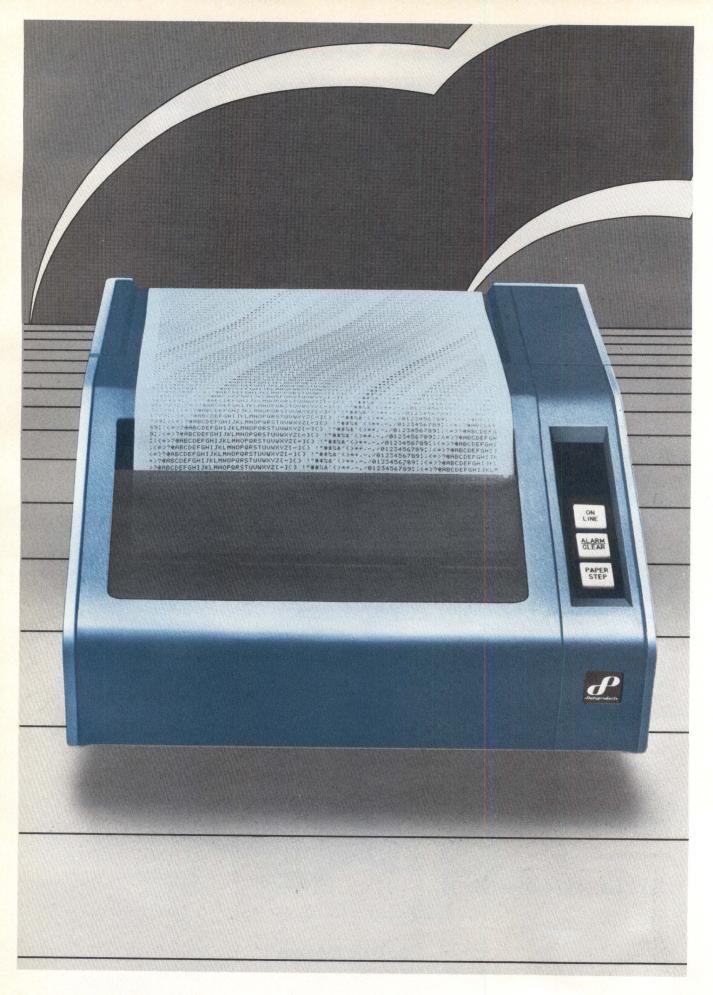
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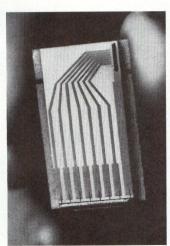
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Concepts of bundled and orthogonal structures are developed and used to place present microprocessor multi-operating level architectures in perspective, as well as to predict future trends

Comparisons and Trends In Microprocessor Architecture*

Edwin E. Klingman

Cybernetic Micro Systems Palo Alto, California

Over the past few years, introduction of literally dozens of microprocessors and hundreds of related devices has presented designers with a wealth of detail that must be mastered for effective design. Manufacturers of these devices have done an admirable job of providing detailed literature concerning their products. What is missing is an overview of the entire microprocessor spectrum and particularly of trends which have evolved and are evolving. Existing literature is largely tabular in nature and simply relates various parameters, such as speed, number of instructions, addressing modes, and registers. Since numerous tabulations are readily available, these details are bypassed and emphasis is placed instead on the microprocessor architectural spectrum in an attempt to detect emerging themes. A thorough understanding of any individual microprocessor, and of interrupt mechanisms in particular, should provide sufficient background knowledge for this discussion.

Concept of Orthogonality

A particularly useful mathematical concept which applies well to microprocessors is that of orthogonality. A system of vectors, ie, multifeature entities, is said to be orthogonal if the entities are sufficiently decoupled; ie, if alteration of a given entity does not necessitate alteration of the other entities composing the system. The concept is almost synonymous with that of independence.

Interrupt Structures as Orthogonal Structures

Probably the simplest example of an orthogonal structure is found in the interrupt system of a computer. The function of the interrupt system is to couple the microprocessor to external systems and to simultaneously decouple the associated response within the machine, ie, make the system's response to a given (interrupting) event completely independent of response to other (independent) events. It should be clearly understood that hardware/software architectural features are being analyzed, ie, the interrupt response mechanism and instructions provided by the manufacturers to effect this decoupling. In any given application, the user may actually contrive a close coupling (in software) between interrupting events. However, there should be no hardware features requiring this coupling. The most extreme decoupling in hardware is achieved by dedicating a separate microprocessor to each process. This is rarely economical or necessary and, to this end, interrupt structures have evolved which allow a given processor to be shared between two or more processes.

If one process is to be suspended while another is operative, it is necessary to save sufficient information to resume the interrupted process with no changes

^{*}This article is adapted from material in the book *Microprocessor*Systems Design by Edwin E. Klingman, copyright 1977 by

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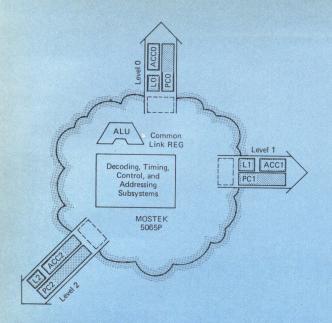


Fig 1 Orthogonal architecture. Extreme example of orthogonal, or decoupled, architecture is provided by Mostek 5065P tri-level machine which saves state of suspended processes "in place" by switching to independent identical machine for interrupting process, later returning to interrupted process

induced by the interruption. This "sufficient information" is classically defined as the state of the system, and considerable attention has been given to savestate/restore-state mechanisms employed to interface two or more operating systems. Since state saving and restoring require finite time, several structures have been designed to optimize this mechanism in terms

of minimal time in transition from one state to another and in terms of minimal instructions required to effect the transition. For example, the Motorola 6800 microprocessor automatically stacks the vector upon receipt of an interrupt and disables the system, restores the state vector, and enables the interrupt system upon execution of the return-from-interrupt (RTI) instruction. This automatic response minimizes both the "change-state" time requirements and the instructions required.

An alternate approach to the multiprocess system may be seen in the Intel 4040, Signetics 2650, Mostek 5065P, RCA COSMAC, Zilog Z80, and other microprocessors. These multilevel architectures approach the problem of optimizing state transitions by minimizing or eliminating the save and restore state vector operations. This is achieved via redundant structures which make it unnecessary to save or restore state vectors. Optimal state transitions are achieved by leaving each state vector "in place" and simply switching to another independent state or operating level. The most extreme development of this multilevel architecture is found in the 5065P trilevel machine produced by Mostek. This machine, consisting of an accumulator, link bit, and program counter, provides a highly orthogonal structure. Linkage between these levels is achieved via an auxiliary link register which is always projected onto the operating level. Fig 1 is an idealized illustration of this system.

Each of the three operating levels possesses software extensions into memory. The degree of orthogonality of such extensions varies greatly. In general, a high degree of independence is desirable in such systems. If the systems have access to common registers, a well-defined access structure is required. (Treatment of this structure, however, is beyond the scope of this article.)

Transition between operating levels in a multilevel system is usually possible under both hardware and software control; ie, transitions may be either gen-

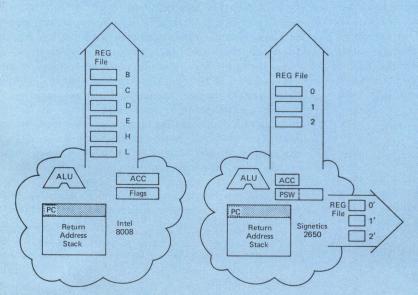


Fig 2 Orthogonal implementation. Signetics 2650 processor represents orthogonal implementation of Intel 8008 architecture. This results in improved interrupt response characteristics and makes available opcode bits which are used to expand addressing modes

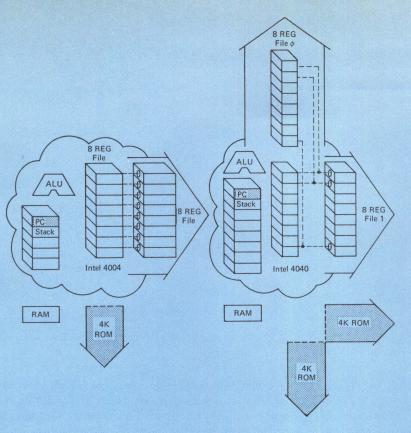


Fig 3 Register expansion. Total number of working registers and program storage registers may be expanded within constraints of existing instruction format by orthogonalizing structure via inclusion of "bank switching" instructions (projection operators). Second generation Intel 4040 utilizes this technique to extend first generation 4004

erated from within a software process or imposed on the system from without.

Orthogonal "Working Files"

A multilevel evolution of the Intel 8008 is seen in the Signetics 2650 (Fig 2). The same basic registerarchitecture is embedded in a different control structure to achieve a radically different total system architecture.

Register file in the 8008 consists of six 8-bit registers designed for scratchpad operations. The same six registers are treated as two 3-register files in the 2650. Only one of these files is accessible by instructions at any given time. A register-select bit in the program status word selects the active file at any given time. This bit may be tested, loaded, stored, set, or reset under program control. The accumulator is always active and available for transfer to or from registers in the active "bank".

System Expansion

Use of orthogonal structures provides optimal state switching for concurrent processing in an interrupt environment. There are additional advantages, as illustrated in the evolution of the Intel 4004 microprocessor. This 4-bit machine, introduced in 1971, uses 8-bit instructions and 12-bit addresses and was the first truly general-purpose processor available as a standard part. The calculator's influence is discernible in some instructions and in the partitioning of the memory. However, the instruction set is general purpose. The 4004

possesses an arithmetic logic unit (ALU), accumulator, program counter, three-deep integral return address stack, and a 16-register file which also functions as eight register pairs. The Harvard architecture, which provides separate stores for instructions and data, can address 4k bytes of instruction store.

The second generation Intel 4040 is upward compatible with the 4004 in the sense that programs which execute on the 4004 will also execute on the 4040. The 4040 has been expanded by extending the return address stack from three to seven deep, and by adding an interrupt facility. Program store has been expanded from 4k to 8k, and the register file has been lengthened from 16 to 24. This has been accomplished within the constraints of the 4004 instruction format via the addition of bank switching instructions that effectively perform a "rotation" of the orthogonal structure. The two systems are schematically represented in Fig 3.

Sixteen of the 4040 scratchpad registers are active at any given time. These registers function in the same fashion as the 4004 register file; ie, either as registers or as register pairs. Registers are normally used for data storage, and register pairs usually function as indirect pointers. There is no necessary connection between the orthogonality of the internal files and that of the two read-only memory (ROM) banks. Either or both of these orthogonal systems can be utilized in interrupt processing. When only one level of interrupt is implemented, "save state" instructions are replaced by the "switch register file" instruction, and one file is dedicated to the interrupt process while the other is used at all other times.

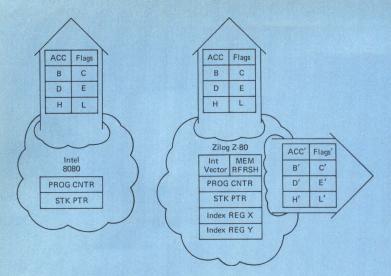


Fig 4 Architecture expansion. Technique illustrated in Fig 3 is used to extend Intel 8080 architecture into Zilog Z80, which possesses both bank switching instructions and bank "swap" instruction which exchanges contents of B, C, D, E, H, and L with B', C', D', E', H', and L'

The ability to extend internal workspace, yet retain compatibility with an existing instruction set, has also been exploited by Zilog in its Z80. This device, with 158 instructions (including all 78 of the original 8080 instructions), possesses a dual register bank (Fig 4).

Variable Dimensionality

Structure of the RCA COSMAC provides extreme flexibility and allows operation in a broad range of system configurations, ranging from 1-dimensional to 8-dimensional. Its 16-register file is highly symmetrical and consists of 16-bit general-purpose registers which may be used as program counters, memory data pointers, or for working storage.

Register functions are assigned under software control, with the exception of the first three registers which may be dedicated to interrupt and direct memory access (DMA) functions. This flexibility is represented in Fig 5. Typical applications of COSMAC utilize configurations intermediate to these two extremes.

System Architecture: Bundled vs Orthogonal

The concept of orthogonality or mutual independence applies to major subsystems, as well as to the operating levels discussed above. An orthogonal subsystem architecture separates every major function into "eigenvector"-like functions which can be scaled with no effect on neighboring functions. The Intel 8080, for example, may be expanded in terms of random-access memory (RAM), ROM, number of interrupt levels, interval times, DMA channels, input/output (I/O) ports, and such, with minimal, if any, cross correlations. In contrast to this, a "bundled" architecture is defined as one in which the extension of any particular resource entails the automatic extension of an unrelated resource. The Fairchild F8, shown in Fig 6, represents

a highly bundled architecture in which the addition of ROM automatically results in the addition of I/O ports, an interval time, and another interrupt port.

The characteristics have been emphasized in Fig 6. A bundled system can always be made more orthogonal by "grafting on" special-purpose hardware, although the basic architecture may make this somewhat awkward. Similarly, an orthogonal architecture may be made less so by including multipurpose chips.

Hardware/Software Orthogonal Extensions

A unique technique of orthogonal expansion has been employed in the Texas Instruments 9900 third-generation processor. Inclusion of an extended operation (xop) instruction allows the designer to add 16 "custom" instructions which may be executed either in special-purpose hardware or interpreted by software. When an xop instruction is executed, the processor checks for the presence of a hardware module and, if present, transfers control to it. An example of such a module is a floating-point processor. When there is no response from the module, the processor traps to one of 16 trap cells located in low memory.

The xop instruction format is shown in Fig 7. The four bits in the operation select code field are used to specify one of 16 extended operations. If hardware modules are present, these bits are decoded (in external hardware) and used to select the appropriate module. If the xop is to be interpreted in software, these bits are used to select the transfer vector in the xop trap space, which consists of 32 contiguous locations immediately following the interrupt trap space. Only one of the options, shown diagrammatically in Fig 7, would be implemented in any given system.

The trap vector points to the new workspace area for the extended operation. The current state (PC, WP, ST) is stored in the new workspace registers, WR13, 14, and 15; and PC and WP are loaded from the trap

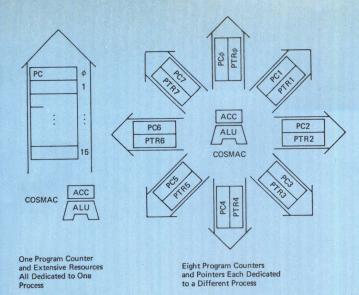


Fig 5 COSMAC architecture. Architecture is flexible and may range from one program counter and extensive resources all dedicated to one process to eight program counters and pointers each dedicated to different process

cell. An XOP status bit is set in the status register, and the source address is calculated from the address fields in the instruction and stored in workspace register 11. The subroutine may then access these data

and execute the special operation. The result should be the same for two systems, one of which possesses special hardware and the other special software. Both options are shown in Fig 8.

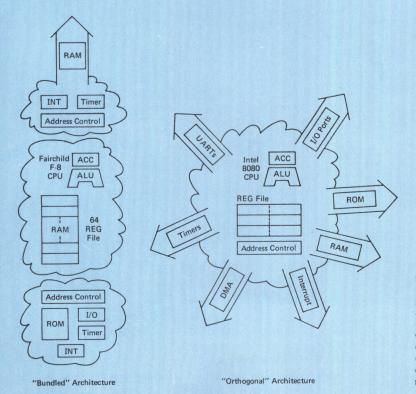


Fig 6 Architectural concepts. Concepts of "bundled" and "orthogonal" architectures refer to ease with which particular feature may be extended. Addition of ROM storage to F8 system usually entails addition of extra I/O circuits, timer, and interrupt and address control circuitry, whereas increased ROM storage in 8080 may be obtained with no effect on other subsystems

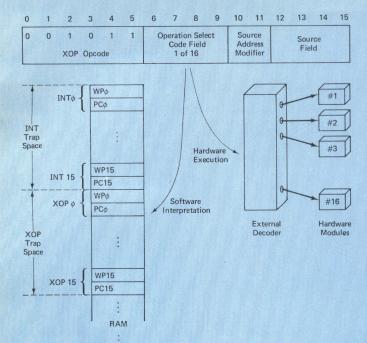


Fig 7 Orthogonal extension. Orthogonal extension of Texas Instruments 9900 is provided via XOP instruction. A 4-bit field in this instruction allows user to specify one of 16 "free" instructions which may be implemented either as subroutine in memory (similar to interrupt service routine) or through external special-purpose hardware

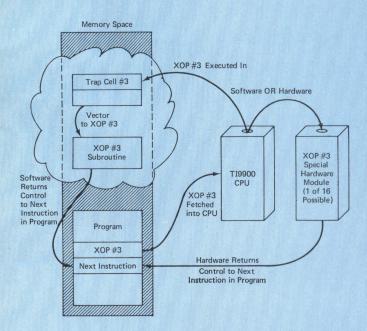


Fig 8 Execution of an XOP. Instruction in the TMS9900 CPU may be executed in hardware or software. If free field has binary number 3 (0011), processor will execute branch to subroutine through trap cell 3 and return data according to user-defined connection. Presence of external hardware may cause execution to trap to equivalent hardware implementation designed to be consistent with subroutine implementation

Major Directions in Digital Design

The direction of microprocessor-related development is largely determined by two factors: user needs and production economics. The first factor is ideally met by custom design tailored to each problem. This customization may be achieved using two approaches. In the first approach, availability of simple, highly orthogonal pieces allows any user to design a custom system which is best suited for the intended application. The hundreds of available medium-scale integrated (MSI) components provide such an orthogonal family. Such systems, if thoughtfully designed, offer easy expansion capabilities at relatively low cost. Disadvantages of such systems generally relate to parts count. The large number of pieces require more board area, consume more power, and are less reliable due to the higher number of connections between devices. The need to design, build, test, stock, and distribute many different parts at relatively low volume means that the economics of mass production are not fully realized.

Custom Devices

3

TO DAY

The second approach consists of designing custom large-scale integrated (LSI) devices which will tailor one-chip systems or subsystems to meet each user's requirements. Although fully automated design techniques may eventually establish this approach as the only viable one, semiautomated techniques are not economically competitive with the orthogonal scheme discussed above. Low volume LSI components are expensive to design, test, and produce—in most cases, prohibitively so.

Programmable LSI

A middle approach between the two customized versions has been taken by LSI designers and has been clearly established as the economically feasible direction for semiautomated design technology. The hardware/software blend is extended into the pieces to such an extent that it is becoming exceedingly difficult to determine just where the software ends and the hardware begins. The perspective in which software is viewed as "on-the-spot rewiring" is fully exploited to optimize all factors required for custom designs, resulting in

Single package—low power, small space requirements, and high reliability

Universal design—one-time design costs and testing amortized over mass-production and distribution

User-selected configurations—10s or 100s of configurations allow low cost custom system design

Special Purpose Processors

Universality of microprocessors as system building blocks derives essentially from their design as general-purpose symbol processors. In order to utilize such free-form or unstructured systems in conjunction with a host of specific control and communications applications, it becomes necessary to formalize certain control and communication tasks. In the same sense that formalization via transistor-transistor logic (TTL) and other specifications led directly to well-defined symbols, and hence to symbol processors, formal specification of control and communications processes leads directly to well-defined tasks and therefore to special-purpose processors.

Tasks and Modes

Although it is relatively easy to define a set of tasks that occur almost universally, it is much more difficult to define a universal mode or method of accomplishing these tasks. For this reason, special-purpose processors which have been designed for given tasks operate in a variety of modes so that they will be as universally applicable as possible. It is through control of the operating mode that system designers customize these processors. This control is effected through mode control instructions sent to the special task processor by the central processing unit (CPU). The number of special task processors exceeds the number of CPUs and is rapidly increasing.

Mode Conrtol of Task Processors

The almost universal requirement of mode control generally has been solved by including in each task processing unit (TPU) a mode control register which is loaded from the CPU with an appropriate control word. In effect, the mode control register in the TPU corresponds to the instruction register in the CPU. The control word is decoded and sets up the data paths and internal operations in the task processor.

Since almost every task involves the transfer or transformation of data, there is also a data register in the TPU. In fact, most such processors provide two registers, one for data out (from the CPU) and one for data in (to the CPU). Many tasks may proceed through a variety of operational states and, therefore, the presence of TPU status information is usually required. A generalized picture of a special task processor is illustrated in Fig 9.

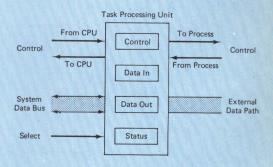


Fig 9 Special task processor. Generalized representation of special task processor includes read/write controls on both processor and peripheral side. Processor writes both mode control information to control register and output data to data buffer. Processor also reads status information from status register and inputs information from received data buffer

It should be noted that, from the perspective of the CPU, each task processor register is an I/O port. (For CPUs with memory-mapped I/O, each task processor register is simply a point in address space.) For example, to output a control word to the task processor, the CPU moves the control word into the accumulator and then executes an output (or write) instruction to the proper port. The port address appearing on the address bus must: (1) select the task processor and (2) select the control register in the task processor.

TPU Summary

Special task processors for handling DMA, interrupt priority and conflict resolution, and parallel and serial I/O are typical examples of orthogonal TPUs. Other TPUs, including programmable interval timers, syn-

chronous data link control (SDLC) chips, cyclic redundancy checkers, hardware floating point and special function chips, and magnetic cassette and floppy disc control chips, are increasing the dimensions of orthogonality and extending the power of the designer. This trend will certainly increase and should lean in the direction of special-purpose unified task processors that provide all required CPU functions on the TPU chip itself. The other direction is toward the totally bundled, unified, general-purpose processor that will provide the universal building block.

The Ultimate TPU

A crucial step in the development of TPUs has been that of programmability. Early TPUs were "semi-intelli-

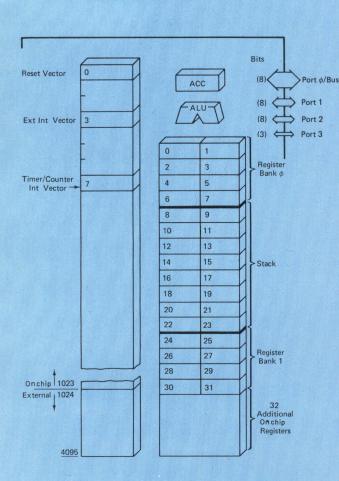


Fig 10 8748/8048 as ultimate microcomputer. Containing all necessary components on one chip, with user-alterable program memory or as ultimate task processor which serves as interface between central processor and external device, the 8748/8048 may be viewed as ultimate microcomputer. Ability of user to program EPROM version allows most custom interfaces to be implemented in this fashion. Both working register banks and program memory banks are highly orthogonal and under program control

gent" units that were programmed by the CPU, as exemplified by the Intel 8257 DMA controller. Although TPUs generally operate under control of a CPU, a natural evolution has occurred which serves to erase the distinction between the general-purpose TPU and the general-purpose CPU. This distinction has almost vanished with the introduction of the Intel 8748/8048 single-device microcomputer and 8041/8741 TPU.

The 8748 is a 5-V only device which includes on one monolithic chip:

CPU—8-bit; with 70-instruction set (21 conditional jumps)

p/ROM—1k x 8 program memory with direct addressing to 4k

RAM—64 x 8 memory contains 8-deep PC stack (may be used for data storage), dual 8-register banks for working files, and is externally expandable to 256 x 8 directly addressable pages

Clock and oscillator—RC or crystal controlled

Power-on clear-extend timing capacitor required

I/O lines—27 TTL-compatible

Jan .

Control lines—5 for extend I/O and memory

Interrupts—external: vector to location 3; interval timer/event counter: vector to location 7 upon overflow Logical AND and OR—directly with I/O ports and conditional branching on test lines

The 8048 is a 5-V n-mos processor with a $2.5 - \mu s$ cycle time and binary and BCD arithmetic capabilities. The 8748 possesses a 1k ultraviolet erasable p/ROM on the chip, while the 8048 uses ROM for mass-production economy. Architecture is shown in Fig 10. Two versions of the chip are the 8048, a microcomputer which serves as a main processor in a system; and the 8041, which serves as an intelligent, programmable, peripheral controller and TPU and which may be used to implement distributed intelligence systems.

The First Three Generations

First generation microprocessors were characterized by slow p-Mos technology, minimal on-chip decoding, and extremely basic architectures. The Intel 8008 typifies the first-generation 8-bit microprocessor. Introduction of the first n-Mos Intel 8080 with on-chip decoding and a respectable instruction set clearly divides the first from the second generation. It becomes more difficult to clearly distinguish between second- and third-generation chips due to the diversity of the available types.

If bipolar (TTL) microprogrammable systems are disregarded and only monolithic microprocessors are considered, the dividing line between second- and third-generation devices centers on the multiprocessor coordination of the National SC/MP and the on-board p/ROM of the Intel 8048, the memory-to-memory architecture of the TI9900, and the compact power of the Mostek 3870 one-chip microcomputer.

The Fourth Generation and Beyond

As LSI packing densities increase, inclusion of special TPU subsystems on the CPU will accelerate. Electrically alterable ROMs on the CPU chip will speed access times and eliminate communication channels between CPU and memory chips, thus freeing more pins for useful I/O functions. The well-developed analog-todigital and digital-to-analog technologies will provide on-chip analog I/O facilities of remarkable power. The economic factors described earlier portend the development of super-bundled general-purpose chips with on-board p/ROMs which may be configured on the spot to particular applications. Speeds achieved with n-Mos technology have already surpassed TTL and the limits have not been reached. Exciting new technologies offer vast improvement in every aspect of microprocessorbased system design.

Conclusion

Two factors—applications which require raw speed and the development of more powerful automated design techniques—argue for the continued development of special-purpose, highly orthogonal hardware. Microprogrammed devices (commonly termed bit-slice machines), such as those available from Intel, AMD, Monolithic Memories, Texas Instruments, Motorola, and others, may best be used to exploit orthogonality. Development of grand scale integrated (GSI) technology will continue the bundled trend toward the universal super-building block computer with analog interfaces on the monolithic chip.

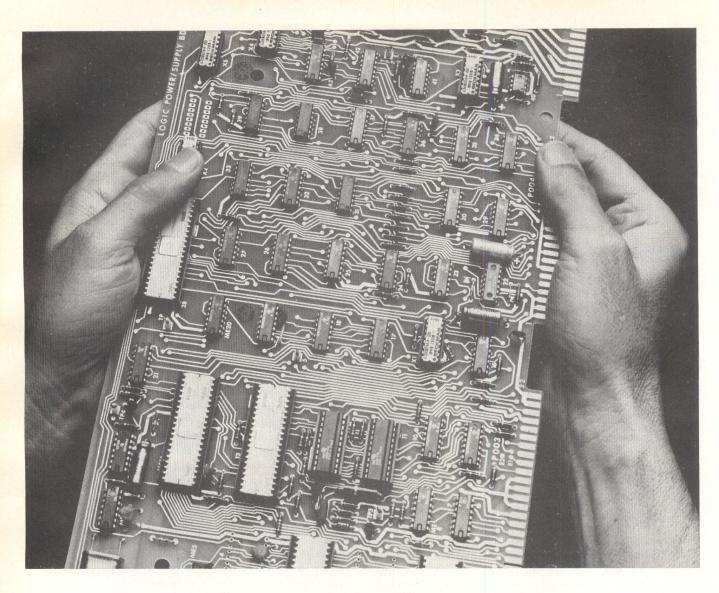
Chip architecture in the foreseeable future will likely be extrapolations of the concepts presented in this article. Although the impact of these chips on system architecture has not yet been felt, it promises to be every bit as interesting as the chips themselves.

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An Update on MOS ROMs

David Huffman

Mostek Corporation Carrollton, Texas

With today's faster, more powerful microcomputer chips emerging in abundance, and larger, more memoryintensive programs being written, semiconductor memory requirements for larger storage capacities, faster access times, and lower subsequent costs have become dominant system design factors. Basic semiconductor memory-chip technology involves variations of randomaccess memory (RAM) and read-only memory (ROM). RAM allows binary data to be written in, and to be read out. New and different programs and data can be loaded and stored in RAM as needed by the processor. Because information is stored electrically in RAM, its contents are lost whenever power goes down or off. When fixed, or unchanging, programs and data are needed by the processor, they are loaded into some form of ROM. In ROM, information is physically (permanently) embedded; therefore, its contents are preserved whenever power is off or interrupted momentarily.

A

Semiconductor memory chips are normally manufactured using either bipolar or metal-oxide semiconductor (MOS) technologies. Bipolar and MOS memories implement bipolar transistor and MOS field-effect transistor (MOSFET) arrangements, respectively, to store addressable sequences of binary 1s and 0s. MOS memories are either static or dynamic. Static memory depends on a dc level for operation; it is easier to implement in many cases, but requires more power. Dynamic memory requires clock signals or level changes for operation; thus more external circuitry may be needed. However, chip size and thus cost is reduced as is power dissipation.

Typically, ROM has been the limiting component in computer system design, operation, and manufacturability. Problems like slow access time, high power dissipation, long prototype and production cycles, and lack of second sources have concerned computer system and equipment designers. This article summarizes the present MOS ROM state-of-the-art and describes the progress made by the semiconductor industry in manufacturing improved ROMs.

ROM Types and Principles

Major types of read-only memory (ROM) are: basic mask programmed ROM; electrically programmable, ultraviolet erasable (EPROM); electrically alterable (EAROM); electrically erasable (EEROM); and field programmable (p/ROM). EPROM is electrically programmable, then erasable by ultraviolet (uv) light, and programmable again. Erasability is based on the floating silicon gate structure of an n- or p-channel MOSFET. This gate, situated within the silicon dioxide layer, effectively controls the flow of current between the source and drain of the storage device. During programming, a high positive voltage (negative if p-channel) is applied to the source and gate of a selected MOSFET, causing the injection of electrons into the floating silicon gate. After voltage removal, the silicon gate retains its negative charge because it is electrically isolated (within the silicon dioxide layer) with no ground or discharge path. This gate then creates either the presence or absence

of a conductive layer in the channel between the source and the drain directly under the gate region. In the case of an n-channel circuit, programming with a high positive voltage depletes the channel region of the cell; thus a higher turn-on voltage is required than on an unprogrammed device. The presence or absence of this conductive layer determines whether the binary 1-bit or the 0-bit is stored. The stored bit is erased by illuminating the chip's surface with UV light. The UV light sets up a photocurrent in the silicon dioxide layer which causes the charge on the floating gate to discharge into the substrate. A transparent window over the chip allows the user to perform erasing, after the chip has been packaged and programmed, in the field. EAROMS and EEROMS use electrical pulses to clear all bits simultaneously.

The p/ROM has a memory matrix in which each storage cell contains a transistor or diode with a fusible link in series with one of the electrodes. After the programmer specifies which storage cell positions should have a 1-bit or a 0-bit, the p/ROM is placed in a programming tool which addresses the locations designated for a 1-bit. A high current is passed through the associated transistor or diode to destroy (open) the fusible link. A closed fusible link may represent a 0-bit, while an open link may represent a 1-bit (depending on the number of data inversions done in the circuit). A disadvantage of the fusible-link p/ROM

is that its programming is permanent; that is, once the links are opened, the produced bit pattern cannot be changed.

Two other types of p/ROM that are not as prevalent in the industry, but deserve mention are EEROM and EAROM. The first, EEROM or electrically erasable ROM, works similarly to the "floating gate" EPROM but can be erased (all bits) by electrically pulsing the device. The EAROM or electrically alterable ROM utilizes special processing techniques that allow bit locations to be reprogrammed at any time. However, unlike a RAM, the write cycle is very long preventing its use as a nonvolatile RAM where both read and write cycles are to be used. Both EEROM and EAROM are used mostly in specialized applications where nonvolatility and electrical erasability are requirements.

In mask-programmed ROM, the memory bit pattern is produced during fabrication of the chip by the manufacturer using a masking operation. The memory matrix is defined by row (X) and column (Y) bit-selection lines that locate individual memory cell positions.

For example, in Fig 1, refer to column C₂ and row 127 as the storage cell location of interest. When the proper binary inputs on the address lines are decoded, the cell at R₁₂₇, C₂ will be selected. If the drain contact of this cell is connected to bit line L², then L₂ will be pulled below threshold, turning off device C₂; note

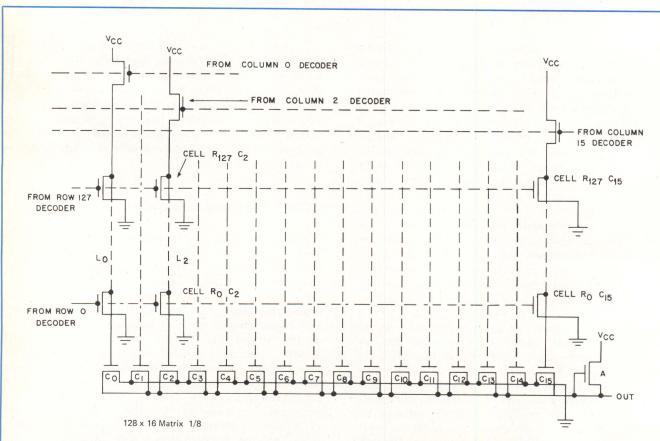


Fig 1 Portion of ROM matrix and output circuitry of MK 34000. If drain contact is made (1 state) when particular cell is accessed, storage transistor will cause OUT line on device A to pull high (to $V_{\rm cc}$). If contact is not made to drain, device will pull OUT line low (0 state)

that devices C_0 , C_1 , and C_3 through C_{15} will also be off since they are not addressed. Therefore, device A pulls the OUT line to V_{cc} for a logic 1 output when cell R_{127} , C_2 is selected.

Alternatively, consider when cell R₁₂₇, C₂ is masked, or does not have a drain contact to bit line L₂. Then, when this cell is addressed, device C₂ is now connected to V_{cc} and will be turned on. Thus, the out line will be pulled to ground through device C₂ and will appear as a logic 0 output. To program a 1 or a 0 into a ROM storage cell, the drain contact will or will not be connected, respectively, to the particular bit line. Note that this type of programming is permanent. An alternative method of performing the same operation would be to eliminate the gate of the storage cell.

Typical ROM applications include code converters, look-up tables, character generators, and nonvolatile storage memories. In addition, ROMs are playing an increasing role in microprocessor-based systems where a minimum parts configuration is the main design objective. The average amount of ROM in present microprocessor systems is in the 10k- to 20k-byte range, while some applications utilize as much as 30k or 40k bytes. Fig 2 shows a block diagram of a typical microprocessor system in which ROM is the predominant program storage element. In this particular application, the 16k ROM is used to store the control program that directs CPU operation. It may also store data that

No at

will eventually be output to some peripheral circuitry through the CPU and the peripheral input/output (P I/O) device.

System Development Cycle

In a microprocessor system development cycle, several types of memory (RAM, ROM, and EPROM or p/ROM) are normally used to aid in the system design. After system definition, the designer will begin developing the software control program. At this point, RAM is usually used to store the program, because it allows for fast and easy editing of the data. As portions of the program are debugged, the designer may choose to transfer them to p/ROM or EPROM while continuing to edit in RAM. Thus, he avoids having to reload fixed portions of the program into RAM each time power is applied to the development system.

Decision making on the part of designer and manufacturer is required during the next step in the development cycle. Depending on the type and quantity of microprocessor systems to be produced, a decision has to be made as to whether ROM, p/ROM, or EPROM will be used for permanent program storage. If only a few systems are to be manufactured, it may be more cost-effective to use either p/ROM or EPROM. EPROM-based storage also allows the main program to be changed

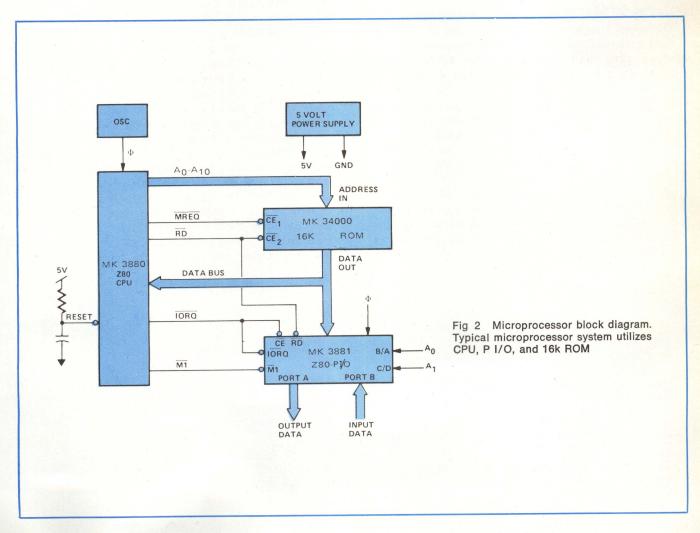
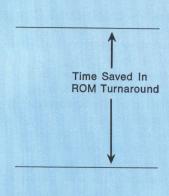


TABLE 1 MOS ROM Manufacturing Process Flow

Wafer Oxidation Nitride First Mask (Gate Mask) Etch Second Mask Implant Polysilicon Third Mask Oxidation Fourth Mask (Contact) Etch Metallization Fifth Mask Glassification Sixth Mask Test Assemble Ship



at any time, even in the field by the end-user. The p/ROM-based system requires replacement; however, it is field programmable. If the main requirement is a minimum parts configuration and many microprocessor systems must be produced, the decision should be to use ROM-based storage.

For many designs, fast manufacturing turnaround time on ROM patterns is essential for fast entry into system production. This is especially true for the consumer "games" market. Several vendors now advertise turnaround times that vary from two to six weeks for prototype quantities (typically 25 pieces) after data verification. Data verification is the time when the user confirms that data have been transferred correctly into ROM in accordance with the input specifications.

Contact programming is one method that allows ROM programming to be accomplished in a shorter period

*Projected cost

of time than with gate mask programming. The step-bystep ROM manufacturing process is listed in Table 1. N-Mos Roms go through basically the same processing steps. In mask programming, most ROMs are programmed with the required data bit pattern by vendors at the first (gate) mask level, which occurs very early in the manufacturing process. In contact programming, actual programming is not done until the fourth (contact) mask step, much later in the manufacturing process. That technique allows wafers to be processed through a significant portion of the manufacturing process, up to "contact mask," and then stored until required for a user pattern. Some vendors go one step further and program at fifth (metal) mask. This results in a significantly shorter lead time over the old gate-maskprogrammable time of 8 to 10 weeks; the net effect is time and cost savings for the end user.

Cost Considerations

Consider a typical microprocessor system and what ROM can provide in terms of cost savings over discrete logic and EPROM. Assume that a single gate function can be replaced with eight to ten bits of ROM and that most of today's transistor-transistor logic (TTL) integrated circuits (ICs) contain on the order of ten functional gates having an average selling price of \$0.40. The typical microprocessor system contains 20k bytes of ROM. Table 2 compares the costs of ROM versus discrete logic.

From the table, one 16k (2048 x 8-bit) ROM can replace 100 to 200 TTL packages. Depending on the total quantity of ROMs required, it can be seen that they are a cost-effective alternative to discrete logic.

Additional savings are possible when ROM is used. Board area is reduced, which lowers material cost; fewer packages reduce insertion costs; and, with smaller boards and fewer interconnections, the cost of incoming inspection is also decreased. When board trouble-shooting costs go down, overall system reliability increases.

At this time, the largest cost-effective EPROM size available is 1024 x 8 bits or 8192 total bits. However, there are many 2048 x 8 bit, or 16k roms available. At an average selling price of \$16/EPROM and \$8/rom, it is evident that rom remains the most cost-effective

TABLE 2
ROM vs Discrete Logic Costs

ROM Capacity (Total Bits)	ROM Cost	Functional IC Gates	ICs	Estimated IC Dollars
8k	\$7 to 8	500 to 999	50 to 99	\$20 to 39
16k	\$8 to 9	1000 to 1999	100 to 199	\$40 to 79
32k	\$16*	2000 to 3999	200 to 399	\$80 to 159
64k	\$20*	4000 to 7999	400 to 799	\$160 to 319

TABLE 3

Important Data Sheet Parameters

General

- Absolute maximum voltage ratings—voltages beyond which parts are likely to be destroyed
- Absolute maximum temperature—operating and storage temperatures beyond which parts may be permanently damaged
- "Recommended" operating conditions—operating conditions that the manufacturer requires for proper operation
- DC parametrics—current and voltage parameters at specified conditions
- Timing diagrams—part timing specifications essential for system design
- Capacitance specifications—particular input and output specifications required to avert drive problems
- Package specifications—pin-outs and package mechanical data for layout and environmental requirements

Specific

- Voltage and current levels—input and output low and high voltage and current levels on all inputs and outputs
- Power supply regulation—detailed power supply regulation specifications
- Output capacitance test value—this value determines maximum number of parts which can be strung together and still meet specifications
- Standby and operate power requirements
- Input and output leakages
- Timing parameters—all timing parameters required to totally specify system operation
- Input methodologies—ROM's truth table should indicate accepted input methodologies including card, tape, or transmit formats
- Operating temperature specifications—should allow for proper system margins after enclosure temperature rises are taken into account

solution. For every two 8k EPROMS, only one 16k ROM is needed. The disadvantage of ROM in small quantities is the mask charge (usually \$500 to \$1000). In larger production quantities, the mask charge is waived when a minimum number of parts have been purchased (typically 500 to 1000 pieces/pattern).

Key Performance

With faster and more powerful microprocessors entering the market, ROM performance is more important than ever, especially since ROM has typically been the limiting factor in system processing speed and operation. When 16k ROMS were introduced several years ago they were fairly slow, with access times ranging

from 550 ns to well over 1.0 μ s. These ROMs made it difficult to take advantage of the full speed capability of newer microprocessors. If processing speed was paramount, the designer usually selected bipolar ROMs, which possess fast speed but have high power dissipation. Density costs are also higher.

Newer Mos Roms (such as the MK34000, 32000, and 36000) provide the system designer with both speed and density. Access time is 300 ns worst case, specified over the full power supply and temperature ranges. In addition, since many microprocessors now have only a single power supply requirement (5 V), the trend in 16k/32k/64k ROM designs is also slanted to this single voltage. Most vendors offer a ±5% supply voltage tolerance and at least one specifies ±10%.

Other Parameters

Many ROM-based memory applications are subject to various detrimental environmental conditions. For instance, an intelligent data entry terminal used on a busy outdoor loading dock could be exposed to vibration-generated electrical noise, extreme temperature variations from -20 to $125^{\circ}F$ (-28 to $51^{\circ}C$), machinegenerated noise, and power line fluctuations. Critical ROM parameters, such as temperature range, input levels, output drive, power supply tolerance, and power dissipation, are being accommodated by innovative memory design and processing techniques to optimize performance and reliability.

Extensive use of ion implantation as a means of controlling circuit zero bias threshold voltages is now prevalent. One ROM vendor uses a substrate bias generator, often called a charge pump which results in much wider operating tolerances. Input levels of 2.0 V, $\pm 10\%$ power supply tolerances, wider operating temperature ranges, faster access times, and lower power dissipation are now available.

Important data sheet parameters that a designer should examine when specifying ROMs are listed in Table 3. Of course, which parameters are important to the individual designer depends entirely on the application. In the loading dock example cited previously, temperature range may be the most critical. In a military airborne application, temperature range and power dissipation would be most important.

Charge Pump Technique

Although the ROM charge pump technique has been utilized for several years, a new design approach has evolved (Fig 3). The charge pump is an on-chip bias generator that is used to shift the thick-field thresholds (V_T) to their proper operating levels, as well as to reduce junction capacitances of the circuit. In dynamic RAMs, an external $V_{\rm BB}$ power supply is used for this purpose. This fixed value bias is useful, as such, but it does not compensate thresholds over temperature. In the MK34000, 32000, and 36000 ROMs (16k, 32k, and 64k, respectively), the charge pump approach does temperature-compensate for thresholds by utilizing a method of V_T feedback. A threshold detector compares V_T values of the circuit with an on-chip voltage refer-

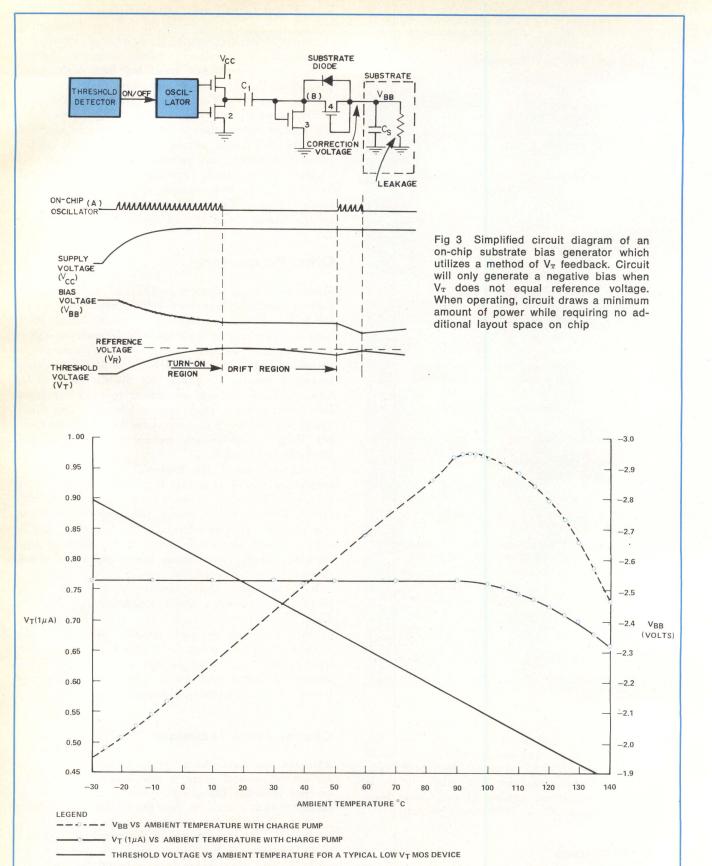


Fig 4 Operating margins. By comparing curves showing $V_{\rm T}$ versus ambient temperature for circuit with and without substrate bias generator, it can be seen that operating margins of a noncompensated device may be quite limited. By utilizing $V_{\rm T}$ feedback method of device operation, $V_{\rm T}$ can be held constant over significantly wide temperature range. Plot also shows $V_{\rm BB}$ versus temperature with generator operational

ence (V_R) . Significantly, V_R is always a fixed percentage of the V_{CC} supply rather than being V_T dependent. Normally, the V_{CC} supply can be held constant over a specified temperature range; thus, the reference will also remain constant, keeping V_T constant. Even if the supply voltage changes, the reference voltage will cause the effective V_T to be within its operating range for a particular supply potential.

The bias generator is actually an on-chip gated oscillator (A) that, when operating, "charges up" the substrate capacitance of the chip with a negative potential. The threshold detector will turn the oscillator on or off if it detects either an inequality or an equality, respectively, of V_R and V_T. This is especially important for V_T versus temperature. Typically, as temperature goes up, V_T goes down; with normal process tolerance included in the total V_T, this could severely limit the allowable specified input levels and temperature range. The threshold detector is sufficiently accurate so that it can compensate for small changes in V_T during normal operation of the part. Fig 4 shows the behavior of V_T, V_{BB}, and compensated V_{TC} over an extremely wide temperature range. The outstanding feature of the compensated V_T curve, is that it is flat over a significant range in temperature. It can be shown that the overall effect is an improvement

TABLE 4
Screening Requirements
Specified for MIL-STD-883, Class B

Test	Method	Condition	Test Level
Visual	2010.2	Condition B	100%
Stabilization Bake	1008.1	Condition C 24 h at 150°C	100%
Temperature Cycle	1010.1	Condition C -65 to 150°C 10 cycles	100%
Centrifuge	2001.1	Condition E 30k Gs YI Plane	100%
Hermeticity			
Fine	1014.1	5 x 10 ⁻⁸ Atm-cm ³ /s	100%
Gross	1014.1	Condition C	
Pre-Burn-In Electrical Test	Static and Dynamic Tests		Mfg's Option
Burn-In	1015 (Dynamic Operating)	Condition D 160 h min at TA = 125°C	100%
Final Electricals	Static and Dynamic per Data Sheet		100%
Quality Conformance	See Mfg's Quality Specification		Sample
External Visua	2009		100%

in system margins, improved yields, and reliability. This is all possible with no increase in chip size and an insignificant increase in power supply current (typically 1 mA).

System Reliability

Replacing many random logic circuits with a single MOS ROM not only makes good economic sense, but also significantly increases system reliability. Printed circuit (PC) board area is reduced along with a multitude of system interconnections. It is possible for a single ROM to eliminate 2000 interconnections when bonding wires and PC board etches are taken into account. This means fewer chances for opens, shorts, and layout problems. When using ROMs, troubleshooting is simplified because there are fewer components, interconnects, and contacts.

In addition, vendors have learned techniques for lowering the power supply current requirements of ROMS. One method utilized is a static matrix with dynamic or "edge activated"* control circuitry. MK32000/36000 ROMS, for instance, draw a typical average current of only 40 mA, compared with 80 mA typical of a comparable density totally static device. When supply current is low, chip temperature is low and reliability is enhanced.

Many vendors now offer enhanced reliability screening as an option. This screening may include temperature cycling for detecting die- and bond-related problems, centrifuging to detect wire bond related problems, and also fine and gross hermeticity testing. In addition, many offer an option on burn-in to weed out infant mortalities. Extended temperature range 16k ROMs are available, as well as devices processed to MIL-STD-883A, Level B. Table 4 lists the 100% screening requirements called out by this specification. While this screening has historically been reserved for military applications, more users are requiring it as a matter of course. Screening of this type means that the user receives the highest reliability possible in his parts.

Standardization

Standardization has resulted in several important advantages. Previously, different pin-out images, various data input formats and media, and different circuit operating modes made system design difficult. ROM vendors have now realized that future product upgrading has significant market value. Also, products that have a second source are more likely to succeed in the highly competitive memory market.

At the present time there are 1024 x 8 and 2048 x 8 bit EPROMS, 1024 x 8 ROMS, 2048 x 8 ROMS, and the newer 4096 x 8 and 8192 x 8 bit ROMS. All vendors sourcing these devices have chosen a standard pin-out configuration (Fig 5) to ease the designer's task in system upgrading.

A designer that implements a standard 8k or 16k EPROM can easily change to an 8k, 16k, 32k, or 64k

^{*}Edge activated is a trademark of Mostek Corp, Carrollton, Texas.

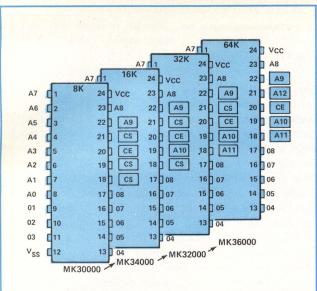


Fig 5 Pin-out sequences. Manufacturers of 8k and larger density MOS ROMs have standardized their pin-out sequences. Significance of these pin images is that they are upgrade pin-compatible with presently available 1024 x 8 and 2048 x 8 EPROMs

ROM by simply using strap options on his standard board. A change from an 8k EPROM to an 8k ROM involves only opening the V_{BB} supply line to pin 21, opening the V_{DD} supply line to pin 19, and altering the function of pin 18 from PROGRAM to CS/CS (see Fig 6). This can be done on either the ROM or the card edge connector. The N/C (no-connect) option available on some 8k ROMs makes even this unnecessary. Upgrading to larger ROMs involves interchanging chip selects and address lines.

Second sources are now plentiful. While performance-compatible ROMs are not always available, vendors are making progress along these lines. Some of the presently available 8k and 16k EPROM pin-compatible ROMs are analyzed in Table 5. The point of the analysis is that the devices listed are basically similar with the same pin-out, method of operation, and general characteristics. Not only do the manufacturers benefit but so do the users.

Standard input formats and media for ROM data have been problem areas. Not long ago, a vendor would accept data only in his format (ie, hexadecimal or octal) and only on card decks. Now virtually any form of transferring data is acceptable. For example, data have been transferred to ROM from media as diverse as telephone data links, EPROMS, and paper tapes. Table 6 lists some examples of the currently available methods of media data transfer. As can be seen from this table, the designer may put his ROM data into essentially any form. The possibility of error is reduced because no conversions of the data need be made to other media to accommodate different vendors.

Conclusions

Turnaround time has been reduced to a tolerable level, pin-outs are being standardized, ROMs are providing larger memory capacity with higher performance, and data are more easily transferred. In the future, the greatest number of applications will most likely be in microprocessor systems. Microprocessor memory requirements continue to increase as control programs get larger and applications become more sophisticated. Concurrently, the microprocessor is becoming higher performance with more control capability, as witnessed by recent 16-bit high speed devices. Today's new generation MOS ROMS are being designed to interface directly and easily while occupying a minimum of space. The

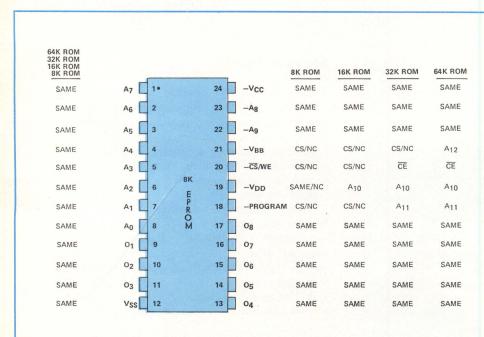


Fig 6 EPROM and ROM pin connection compatibility, Virtually all pin connections are same for an 8k EPROM through a 64k ROM. Significant difference occurs on the EPROM VBB, V_{DD}, and program pins. These pins in ROM are either CS/CS functions or address inputs with allowing some manufacturers no-connect options. With N/C option. EPROM can be directly replaced by ROM with no circuit change, except when using 16k or larger

TABLE 5
Comparison of Several Available 16k ROMs

Parameter	Mostek MK 34000	American Micro Systems S6831B	General Instruments R03-9316A/B	Intel I2316E/8316E	Motorola 68316E	Synertek 2316B
Input Voltage High (V _{IH}) Low (V _{IL})	2.0 V min 0.8 V max	2.0 V min 0.8 V max	2.2 V min 0.65 V max	2.4 V min 0.8 V max	2.0 V min 0.8 V max	2.0 V min 0.8 V max
Output Voltage High (V _{OL}) Low (V _{OL})	2.4 V at 220 μA 0.4 V at 3.3 mA	2.4 V at 100 μA 0.4 V at 2.1 mA	2.2 V at 100 μA 0.45 V at 1.6 mA	2.4 V at 400 μA 0.4 V at 1 mA	2.4 V at 220 μA 0.4 V at 1.6 mA	2.4 V at 200 μA 0.4 V at 2.1 mA
Power Supply Current (Icc)	60 mA max 30 mA typ	TBD max 30 mA typ	110 mA max 90 mA typ	120 mA	130 mA	98 mA max typ
Output Leakage Current	10 μΑ	10 μΑ	10 μΑ	10 μΑ	10 μΑ	10 μΑ
Input Leakage Current	10 μΑ	2.5 μΑ	10 μΑ	10 μΑ	2.5 μΑ	10 μΑ
Power Supply Voltage	5 V ±10%	5 V ±5%	5 V ±5%	5 V ±5%	5 V ±5%	5 V ±5%
Access Time Referred to Addresses	350 ns	450 ns	450 ns	450 ns	500 ns	450 ns
Chip Select To Output Delay Time	175 ns	200 ns	200 ns	120 ns	300 ns	250 ns
Chip Deselect To Output Delay Time	150 ns	150 ns	200 ns	100 ns	175 ns	250 ns
Operating Temp Range	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
Extended Temp	Yes	Yes	Yes	NA	Yes	NA

TABLE 6
Acceptable Format and Media
For Input of ROM Data

Format	Media
Mostek	Card Deck
National	Paper Tape
Fairchild	ROM
Intel Card	p/ROM
Intel Tape	Data Link
Electronic Arrays	
Mostek F8	
Motorola 6800	

importance and necessity of ROMs to system design have resulted in a continual effort by the semiconductor industry to improve performance, reliability, and cost.

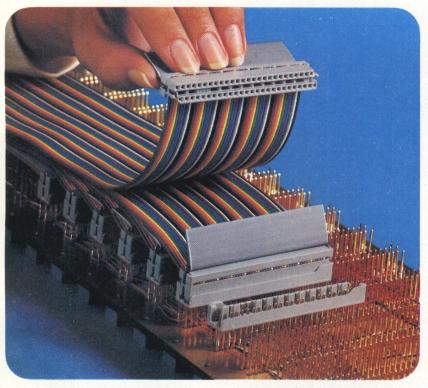
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Dave Huffman holds a BS degree in electrical engineering from Purdue University. Currently an application engineer at Mostek, his experience includes work in the areas of ECL process development, CMOS product engineering, linear circuits product marketing, and in solid-state physics.

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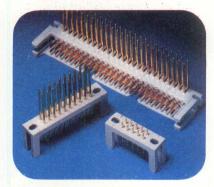


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A low cost, dedicated microprocessor diagnostic tester accommodates both factory testing and field service troubleshooting by providing testing versatility with high uniformity in a portable unit

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Microprocessor servicing can be achieved effectively with a diagnostic tester designed specifically for the system under test. Available microprocessor test systems, such as commercial card test equipment, are complex, expensive, and cumbersome because of the intricate test pattern generation tasks, the highly skilled labor, and the large equipment size. Microprocessor in-circuit emulators are extremely useful for engineering design and certain manufacturing test cases; however, they represent a partial overkill and are time-consuming for most field service diagnostic work. More importantly, both in manufacturing and in field service, it is desirable to utilize a highly automatic test method. For most microprocessor systems, it is not economically feasible to include excess capacity for self-diagnosis because of the cost. Therefore, a low cost portable diagnostic tester designed specifically to check out a particular microprocessor represents an effective solution to versatile performance, test uniformity, and reasonable price. A unit of this type offers the user such benefits as

Portability—small size and light weight make it ideal for both factory and field service

Economical manufacturing testing—relatively low production cost and large cost savings are obtained over general-purpose test equipment that usually does not perform dedicated functions as well

Test versatility—software resident in programmable read-only memory (p/ROM) allows versatile tests and eases the introduction of required changes to the tests

Test uniformity—tests and test environment remain the same, ensuring checkout repeatability both in the factory and in the field

Functional Description

A typical microprocessor system (Fig 1) consists of read-only memory (ROM or p/ROM), random-access memory (RAM), and peripheral devices. It is assumed that one of the peripheral devices is some type of output device, which is most often the case. The diagnostic tester for this system must share the central processor unit (CPU) address bus, data bus, and appropriate CPU control signals. Once these buses are operational, the diagnostic tester can exercise the microprocessor and cause execution of tests upon any device on the CPU bus. Note that to the microprocessor the diagnostic tester is merely additional memory and input/output (I/O); therefore, the system designer must provide addresses for the tester to communicate with the system.

Fig 2 is a block diagram for a portable 8080 diagnostic tester. (Diagrams using other types of microprocessors would be similar.) The 16-bit system address bus is buffered and driven on to the test interface board and is used to address the ROM (or p/ROM), RAM, and I/O control lines. Amount of ROM required depends on test complexity and number of tests desired. Typically, 4k to 8k bytes of ROM or p/ROM are adequate. In addition, 1k to 4k bytes of static RAM can be used, thereby eliminating the requirement that the system RAM be functional.

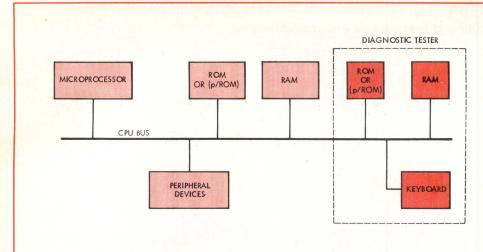


Fig 1 Typical microprocessor-based system. System consists of many devices, all sharing common CPU bus, which is made up of address bus, data bus, and associated handshake control lines. Devices sharing CPU bus are microprocessor, p/ROM, RAM, and peripheral device interfaces. Note that diagnostic tester is simply additional memory and peripheral devices

A 25-key calculator keyboard, which the CPU can read in three 8-bit bytes of data via the system data bus, provides convenient and readily available user inputs and control. Table 1 indicates typical keyboard key assignments. Some keys may be assigned more than one function. In this case, of the available keys, 24 are assigned in three 8-bit bytes. This necessitates assigning three 1/0 addresses to the keyboard interface.

Although these assignments are typical of those for most diagnostic tester applications, certain specific designs may require special key functions.

The keyboard interface is composed of a 1-of-3 byte multiplexer which selects eight keys at a time and gates them on to the data bus when the microprocessor scans the keyboard. This makes it necessary for the software to provide the key debounce function. One

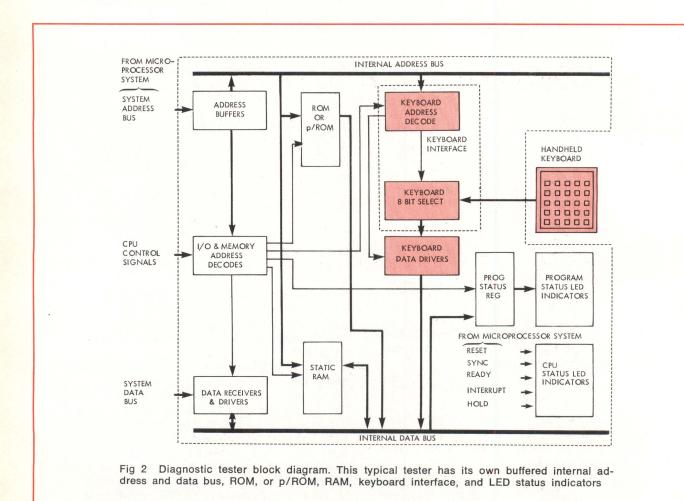


TABLE 1 Typical Keyboard Assignments

Mnemonic	Function	Manual	Allows manual loading of registers or memory with any desired hexadecimal data value
Enter	Initiates commands or permanent storage of data values and test numbers	Error Wait	Sets a flag that causes the test program to wait after a test failure has occurred.
Reset	Returns the operator to the command entry mode so that new diagnostics may		Depressing the Continue key restarts the test until another failure is detected
	be initiated	Register	Selects register diagnostic tests
Continue	Continue Causes continuation of a test which is waiting for operator-response before con-	Memory	Selects memory diagnostic tests
	tinuing execution	Run	Causes the previously selected diagnostic
Sequence	Sets a flag which allows tests to se-		test to be executed
	quentially execute in numerical order until all tests have been run	0 to 9, A to F	Enters corresponding hexadecimal data symbol

Loop

method which can be used is illustrated in Fig 3. This algorithm incorporates leading edge and trailing edge pulse detection. A key must be depressed a minimum of 5 ms and then released a minimum of 5 ms before conversion to a coded character for selection of the desired function or test. Approximately 100 bytes of ROM or p/ROM must be allocated for scanning and debounce functions. Upon debouncing and decoding the

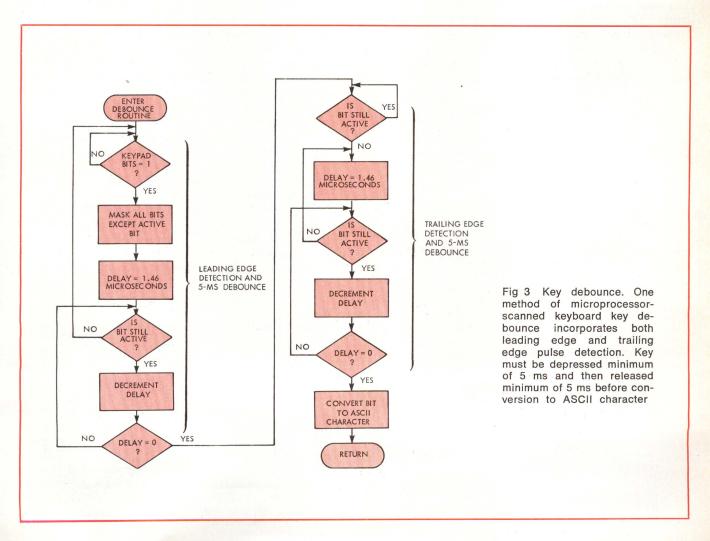
A

key depressions, tests may be run on other peripheral devices, data may be entered into memory or peripheral devices, or flags may be set. In fact, almost any test that can be run using keyboard input is feasible.

Sets a flag which causes the selected diagnostic test to be run repeatedly until

the Reset key is depressed

An 8080 diagnostic tester presently in use is shown in Fig 4. This tester consists of a large, densely populated printed circuit (PC) board connected to a hand-



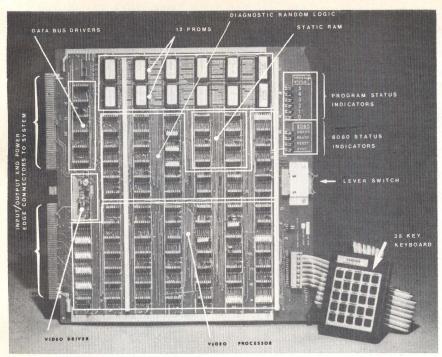


Fig 4 Diagnostic tester board. Typical diagnostic tester illustrates different areas of hardware. Approximately half of tester board consists of video processor and driver which allow output to existing raster-scan CRT display

held keyboard, and weighs approximately 2 lb (0.9 kg). The tester board includes memory (both p/ROM and RAM), a keyboard interface, program status registers and indicators, and address, control, and data circuitry. The diagnostic tester card shown in Fig 4 is currently used with Ramtek graphic display systems that drive raster-scan cathode-ray tube (CRT) displays. The lever switch allows selection of any one of the system refresh memories for outputting diagnostic test results to the CRT displays.

Light-emitting diode (LED) displays are used to indicate program status. Typical status displays and their respective functions are listed in Table 2. These displays indicate what operator response is required, and

TABLE 2
Typical Program Status Displays

LED	Mnemonic	Function
0	On Line	CPU is executing from ROM or p/ROM on diagnostic tester board
1	Enter Command	CPU is waiting for command entry from keypad
· 2	Enter Data	CPU has previously received command entry and expects data entry from keypad
3	Test in Process	CPU is executing selected test
4	Test Wait	CPU is waiting for operator to depress Continue key
5	Unassigned	User option

the sequence of program execution. Status indications such as enter data, enter command, test in progress, and test wait are a few common uses. It is also convenient to use LEDs to indicate CPU status, including the reset, ready, sync, and hold lines. These status indicators can display critical handshake lines, clocks, and hung states. For instance, a DMA-initiated-but-not-completed signal will cause the hold line to be on continuously. These displays should be mounted at the edge of the diagnostic test interface board for operator visibility and are mandatory for efficient troubleshooting.

There are many types of input devices that could be utilized, but a handheld keyboard has the significant advantages of low cost, high versatility, small size, and light weight. Some sort of output device is normally required and usually is a part of the microprocessor system under test. By using a serial port, a variety of I/O devices can be utilized compatible with the specific microprocessor system. Assuming that a card slot within the chassis will be dedicated to the diagnostic tester, the only cables necessary are the keyboard cable and a serial (I/O) interface cable, if included.

Tester Design Considerations

For optimum test versatility and uniformity, a microprocessor should be hardware-designed to facilitate factory testing and field service troubleshooting. This means that from a hardware viewpoint, servicing requirements considered early in the microprocessor system design phase will greatly reduce checkout problems encountered later during the diagnostic tester design. An extra PC board slot and connector should be dedicated on the microprocessor for the tester connection, and appropriate microprocessor bus and handshake lines should be available at that point. These considerations include CPU status lines, interrupt lines.

serial ports, and other signals pertinent to the microprocessor system. Frequently, an existing board in the system already contains the required signals and may be easily removed and the tester board substituted; however, a separate test board slot is usually a better solution. Many times a microprocessor system is rendered inoperative because of a very basic fault. CPU status indicators can give immediate indications as to what the system is doing. Since these indicators are incorporated into the diagnostic tester, the system backplane must accommodate these signals at the tester slot.

Another test problem to be anticipated is the speed at which the microprocessor system operates. Some p/ROMS or ROMS will be too slow, depending on microprocessor clock frequency. Certain p/ROM or ROM access times are too long to satisfy microprocessor reader cycle requirements. For example, ultraviolet erasable p/ROMS are valuable for developing software for a system; however, they may not be fast enough to run real-time tests. One solution is to use equivalent bipolar ROMS which are faster; another possible solution is to drive the ready line for a microprocessor wait state. Although the latter will not allow the microprocessor system to run at full speed, it may be acceptable. Note that provision for an address range for the ROM in the diagnostic tester must also be considered.

Keyboard scanning, key debounce, and required tests must all reside in the specified range of addresses. Additionally, it is recommended that 2k bytes minimum be allowed for overhead software. Since a nominal excess of ROM is desirable, it is recommended that a reasonable amount of (initially) unassigned ROM be provided for contingency purposes. Typically, 2k bytes

are adequate.

Another consideration is how to cause the CPU to execute instructions from p/ROM-resident software on the diagnostic tester instead of from normal product memory, and thus gain control of the CPU for the tester. One possibility is a Test/Run switch located in the microprocessor system. Upon a system reset or shortly after power-up, the CPU reads the switch position and executes a branch to the diagnostic ROM if it is in the test position; this concept is illustrated in Fig 5. Another possibility is a switch on the diagnostic tester which can interrupt the CPU. This is not as desirable since it requires both CPU and interrupt system to be operational, and the interrupt system, which may be malfunctioning, adds another level of complexity. A third approach is to implement a switch that controls the address definition for part of the system memory and the diagnostic tester. In this case, the tester memory would be switched to begin at address 0 and the CPU would be reset to begin execution at address 0, which is the diagnostic test function.

Diagnostic Strategy

The usual sequence of operation for diagnostic testing any microprocessor system is

- (1) Insert or connect tester to system, and initiate operation
- (2) Test CPU and buses for operation. If program status indicates negative, change CPU and/or buses

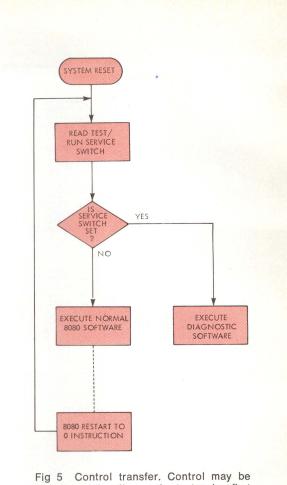


Fig 5 Control transfer. Control may be transferred to diagnostic tester by first using service switch and then initiating system reset. Another method is to execute an RST0 instruction which restarts microprocessor at address 0

(3) With CPU and buses operational, perform simple diagnostics first. Then perform more complex operations until system is tested completely or fails

Since the diagnostic tester uses a scanned keyboard as an input device, it is not limited to any particular group of tests. For example, by changing software within a p/ROM, a test can be written in any particular manner selected. A simplified register test (Fig 6) will march a bit pattern through a memory or register and read after each write to verify contents. The error print routine could utilize an index table so that the exact register or memory chip could be pinpointed. Software in the p/ROM can be changed (by interchanging p/ROMs), and thus, using a scanned keyboard, the meaning of particular keys may be changed. An extremely versatile configuration includes a serial port that can drive a teleprinter terminal, or, alternately, a model that provides remote troubleshooting capability. Test versatility of a diagnostic tester appears to be limited only by the creativity of the designer and the programmer.

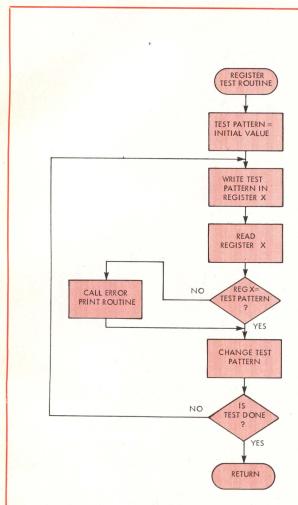


Fig 6 I/O register test. Basic register test flowchart illustrates how microprocessor may test an I/O register. Test pattern value is written into I/O register or read-write memory. Then, contents of register or memory are read back to microprocessor and are compared against pattern previously written. All bits may be tested by changing test pattern written into register or memory

A few specific tests include those on different types of memory, register, DMA, interrupt, and I/O devices. In addition, diagnostics can be written to use available output devices, such as teleprinters, printers, plotters, or CRTS, without necessitating expensive support equipment. Test function modes which are usually very helpful are

Manual mode—allows the user to load a particular value at a specific address

Loop mode—continuously executes a particular test

Sequence mode—sequences through all tests in a predefined order until a fail is encountered or all tests are completed These modes are flag bits which are activated prior to entering the diagnostic test and are reviewed during execution of diagnostic routines. For example, in Fig 7, the loop mode flag is tested at the end of each diagnostic test. If the loop flag is set and the reset key is not depressed, the diagnostic test routine is automatically re-entered and repeatedly executed. By means of a portable diagnostic tester, the test technician, customer, or field service engineer can run a multitude of system tests and exercise almost every aspect of the microprocessor system. The benefits of diagnostic testing are especially applicable to initial system debugging, test versatility, and test environment uniformity.

Manufacturing Testing

For manufacturing testing, the only precaution in using the diagnostic tester is that the user must make the assumption that the microprocessor buses are operational and that the CPU can execute instructions from the tester memory. If these requirements are not met, the initial testing sequence of a microprocessor system is to bench-test CPU, address bus, data bus, and handshake lines using a microprocessor in-circuit emulator for initial system debugging. The emulator simulates the CPU and provides repeated continuous I/O and memory transfers within the system under test even though the system is inoperative. Then, when CPU buses and handshake lines are operational and the microprocessor can read the tester memory, the diagnostic tester is used for higher system level testing or specialized testing of a particular subsection (PC card) of the system. For example, a complex memory test pattern can be conveniently run on memory boards with diagnostics.

Factory test stations can be generated by utilizing a copy of the microprocessor-based product in conjunction with a diagnostic tester. If volume production is required, each different card within the microprocessor system can have a corresponding dedicated test station that incorporates a single diagnostic tester design and utilizes appropriate software (ie, a memory card test station or an I/O card test station.) The same test software generated for the factory can be utilized by field service; this results in considerable savings and provides uniformity of test method and test environment.

Field Service Support

Field service personnel usually realize the greatest advantages from a portable diagnostic tester, since the same tests that were run during manufacturing test can be duplicated in the field without expensive support equipment. Not only is the diagnostic tester a valuable aid in acceptance of newly installed equipment, it also offers field service personnel a quick means of problem analysis. This can save valuable time in deciding whether to interchange a circuit card or fix a component problem.

Often field service personnel are unable to begin repair of their equipment immediately because other

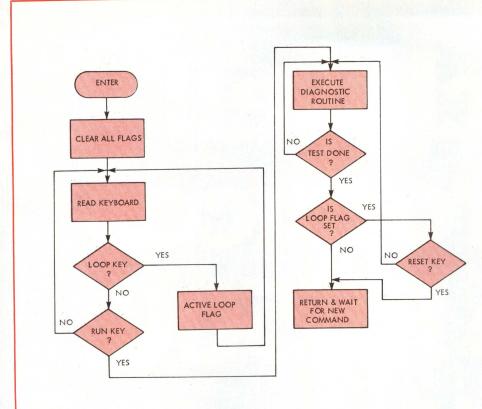


Fig 7 Loop mode relationships. Flowchart illustrates relationship between loop mode, reset, and diagnostic test. Depressing loop mode key will activate loop flag. Upon completion of diagnostic test routine, loop flag is tested and, if set, the microprocessor will rerun test routine until reset key is depressed. If loop flag is not set, microprocessor returns to keyboard scan mode and awaits new command

associated test equipment is unavailable; in contrast the diagnostic tester turns the microprocessor-based system into a standalone test environment. Although it is most advantageous to use an existing form of output available to the microprocessor-based system, such as a printer or CRT, a serial I/O port can be incorporated with a small printer to provide output. Another interesting concept is to connect a modem to a serial port which is part of the diagnostic tester. This allows the system to be interrogated or tested remotely over telephone lines from the factory. Special test programs can be transferred into RAM on the diagnostic tester to aid in troubleshooting more complex problems. Fitting easily into a field service kit, the tester combined with a few spare PC boards can provide field service capability for failures in excess of 95% in some systems. If the CPU is inoperable, the tester will indicate this fact using appropriate status indicators.

achievable with modem connections. The concept of troubleshooting down to the IC chip with a diagnostic tester has become a reality. Memory tests can be run that will determine and print out the location of the faulty IC.

A properly designed portable diagnostic tester can provide sufficient advantages to make a microprocessor-based product attractive to the customer. Inherent cost savings and outstanding tester performance also offer substantial benefits to the manufacturer.

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Conclusion

Many different techniques and kinds of equipment are available to implement efficient microprocessor system diagnostic testing. The portable type of diagnostic tester can provide factory, customer, and field service personnel with an efficient means of isolating failures or validating microprocessor system operation. In addition, remote troubleshooting using telephone lines is



John William Neese, an engineering assistant on the engineering staff at Ramtek, has had extensive experience in microprocessor development systems, and is currently interested in microprocessor controlled system analysis. He is an engineering student at the University of California, San Jose.

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An Interactive Software Program for a Standalone Graphic System

Robert I. Ross

Tektronix, Incorporated Beaverton, Oregon

Interactive capabilities of this software program allow analysis of circuits by building them from interconnected 2-port parameters for subsequent outputs in tabular and graphic forms on various types of grids

Over the past few years many circuit design and circuit analysis software programs have been developed for design engineers. Typically, the user accesses these programs via a timesharing system. Timesharing services offer several advantages: large amounts of data storage are available, the programs are powerful, and they are continually updated.

However, there are disadvantages. A user who does not have extra peripherals or a sophisticated terminal may not be able to take advantage of the more powerful programs. Some resident programs might have a severely limited output format. Another common timesharing system user complaint is that system reliability is low. Finally, timeshare charge schedules are often obscure.

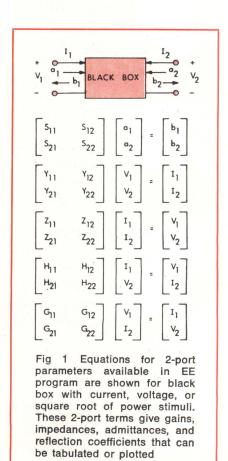
Standalone Graphic System

The Tektronix 4051 graphic system is specifically designed as a standalone device aimed at overcoming the stated timesharing program deficiencies. This system can be configured with up to 32k bytes of resident memory, and will also accept a mag-

netic tape cartridge that has a 300k-byte capacity. System software is stored on a magnetic tape cartridge. One unique program available with this system for circuit analysis and circuit design is Plot 50: Electrical Engineering, Volume 1 ("EE program," for short). There is enough room in the system memory to store the EE program, device data, analysis results, and program that describes the analysis.

An advanced feature of the system is that it can give both tabular and graphical outputs. Graphical capability is important because most electrical engineering analyses call for graphs since they are the easiest way to represent data.

The system's large resident memory and auxiliary magnetic tape storage let the user handle very difficult problems. It can accept inputs from 25 devices, each providing 2-port parameters measured at as many as 30 frequencies, and can make calculations for up to 150 frequencies for one analysis. The system stores the results on magnetic tape, and can display them on a CRT.



Special-Function Keys

Special-function keys on the graphic system keyboard simplify operations for the user. These keys provide routines that enter and edit codes and data. Consider a typical user circuit analysis sequence. The user first enters the "code" that describes the circuit and the analysis desired. If errors are made while typing in the code, the user can edit with a special-function key.

All special-function keys perform operator-related services. For instance, the user may want to store the edited code; enter and store devices for his circuit in terms of 2-port parameter data; or start the analysis that the code specifies. There is an individual key for each of these functions. The remaining keys access some major routines in the system. Some examples are plotting or listing analysis results, and transferring data to an optional data tape.

Advanced Capabilities

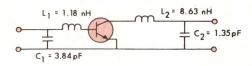
The EE program offers several advanced capabilities. Among the outstanding ones is the interactive format (in which the program asks questions and the operator answers), making it easier for the user to follow through the program. Consequently, this standalone graphic system can provide complete hardware-software integration with a high degree of versatility, while still maintaining the power of timesharing systems.

Only one peripheral is needed—a hardcopy unit that will make a permanent record of the listings and plots displayed on the CRT. Since the EE program automatically draws grids for graphic displays, special graph paper is not needed for any X-Y plotter connected to the system.

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The EE program represents other advances in electrical engineering software. One feature is the ability of the program to strip away components or networks as well as add them. Thus, the system can correctly represent an intrinsic device or circuit with the parasitic lead lines or test fixture mathematically removed. If the user knows (from measurement data) the overall circuit response at one part of the circuit, he can derive the response of the remainder of the circuit.

Another advance is the ability to change the configuration of 3-termi-



LIST CODE

1: FR FS 1 3 .1 FS 4 10 2:
2: CP 3.84 CA
3: LS 1.18 CA
4: DAT 1 CA
5: LS 8.63 CA
6: CP 1.35 EQ
7: NEX
8: S11S

CODE LENGTH= 86. SIMPLE DIAGNOSTIC (Y OR N)?

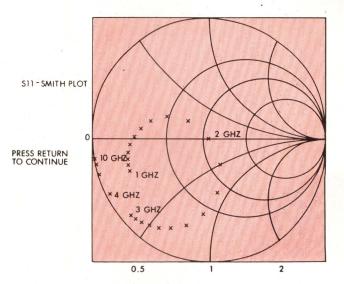


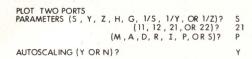
Fig 2 Example showing code used to plot $S_{\rm II}$ Smith Chart for transistor with matching networks. Line 1 specifies frequencies from 1 to 3 GHz in 0.1-GHz steps and 4 to 10 GHz in 2-GHz steps. Lines 2 through 6 specify cascaded components including transistor 2-port parameters contained in DAT 1. EQ step accumulates overall 2-port parameters; NEX step marks end of frequency loop. Line 8 instructs terminal to plot $S_{\rm II}$ on Smith Chart, as shown

nal, 2-port devices; the user can switch transistors specified in a common-emitter configuration. The configuration change routine can also be used to analyze standard circuits that are hard to represent with conventional 2-port analysis (such as differential amplifiers and Darlington pairs).

Program Analyses

The EE program exemplifies major advances in graphics software that

have appeared recently. A detailed examination reveals some interesting circuit analyses possible with this computer-aided design program. Circuits are analyzed by building them from interconnected 2-port parameters, the familiar S, Y, Z, H, and G terms that express relationships between input and output variables. This method contrasts with the conventional nodal approach for specifying circuits in computer analysis, where each node is numbered and the



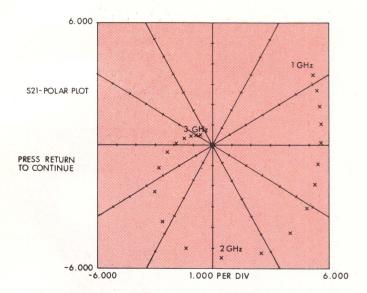


Fig 3 S_{21} is plotted on polar grid using interactive mode for circuit shown in Fig 1. Note that third question "(M, A, D, R, I, P, or S)?" is asking for magnitude, angle, dB, real or imaginary components, and polar or Smith chart presentations

interconnection of components is described in terms of these numbers.

An advantage of the EE user-oriented program is its ability to display results of an analysis quickly and easily in many forms and on many types of grids. It is highly interactive and very versatile, and can also be set up so that the analysis is completely automated.

2-Port Techniques

Use of the 2-port method of circuit specification is familiar to high frequency and microwave design engineers, who are typically concerned with scattering parameters (S parameters). The 2-port method provides them with information such as stability factor, maximum available gain, and stability circles.

The 2-port techniques are also useful for conventional ac circuit analy-

sis. An advantage is that the information provided by the Y, Z, H, and G parameters is directly available in the form of voltage gains, current gains, impedances, and admittances, ie, the very terms that design engineers customarily use. As an example, input impedances can be obtained from Z₁₁ or H₁₁ (the latter represents input impedance with the output shorted, whereas the former is the input impedance with the output open). H₂₁ gives current gain, and G₂₁ gives voltage gain (see Fig 1). Parameters 1/S, 1/Y, and 1/Z are also available. These are element-byelement reciprocals of S, Y, and Z, respectively (eg, the 11 term of 1/Y is simply $1/Y_{11}$).

Various 2-port parameters are mathematically related so that results of one set can be conveniently expressed in terms of another. The defining relationships are given in terms of a "black box" device with external stimuli of currents, voltages, or square roots of power (Fig 1).

Program Coding

Parameters used in the program are 2-by-2 matrices, with each entry a complex number. Unless a certain device is to be specified as a table of 2-port parameters, the user does not need to be concerned with two ports. The program has a large library of components, including resistors, capacitors, inductors, controlled sources, and transmission lines, which are entered by the user as actual devices and converted internally to two ports. To construct a circuit, the user specifies these devices and how they are connected together. When the program is executed, 2-port parameters for the overall circuit are found by mathematically combining the specified components; the final result is a set of 2-port parameters (Fig 2).

Output Presentations

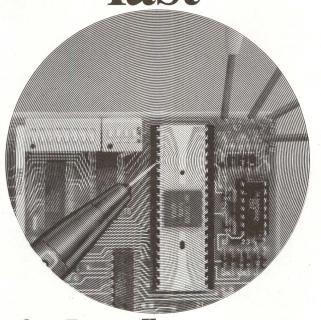
Analysis is often desired over a range of frequencies, which conveniently lends itself to a tabular or graphic format. Output variables are complex numbers; information about them that can be obtained from the program are magnitude, magnitude in dB, and real and imaginary parts.

Normally, if a sequence of graphs or tables is desired, only one tabular output or plot at a time is displayed for the user to view and/or copy. However, there is also a "copy" option that allows the entire sequence to be presented and copied automatically without user intervention.

Alternatively, the user may opt to employ the more versatile interactive mode, in which he may specify the organization of each tabular output or plotting routine. A dialogue format is used, and once all questions are answered, the 2-port results (which are stored on the tape cartridge) are presented as specified. An example of interactive plotting is shown in Fig 3.

Polar presentations are possible with polar grids, and in the case of S or 1/S parameters, with Smith grids. For rectangular grids, the axis may be linear or logarithmic. Autoscaling is used in most cases. Thus, the graph could have been coded in an output specification at the beginning and plotted automatically.

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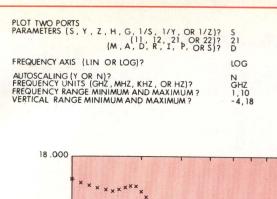
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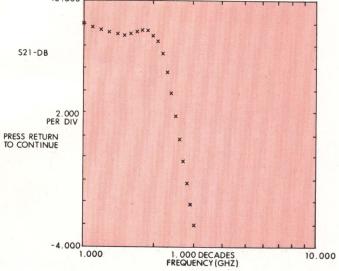


Fig 4 Magnitude of S21 in dB is plotted using manual scaling to magnify low frequency end of response

However, an advantage of using the interactive mode is that plots can be manually scaled.

Manual scaling is useful for two major reasons: it provides a method of limiting the data to be plotted so that a portion of the results may be focused upon; and it lets the user choose a grid larger than that selected automatically so that, for example, axes of several graphs may be standardized for overlay. Also, the user is able to specify the frequency units of the axis in a rectangular plot. Fig 4 illustrates the results of manual scaling for an S_{21} plot.

Summary

The EE software program, in conjunction with the 4051 graphic system analyzes circuits based upon 2port parameters that define input and output variables. Circuit results are displayed in tabular and graphic formats. A special-function keyboard permits the user to enter, edit, and store code and data; select circuit analysis sequences; and choose different output presentations.

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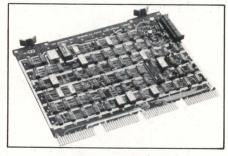
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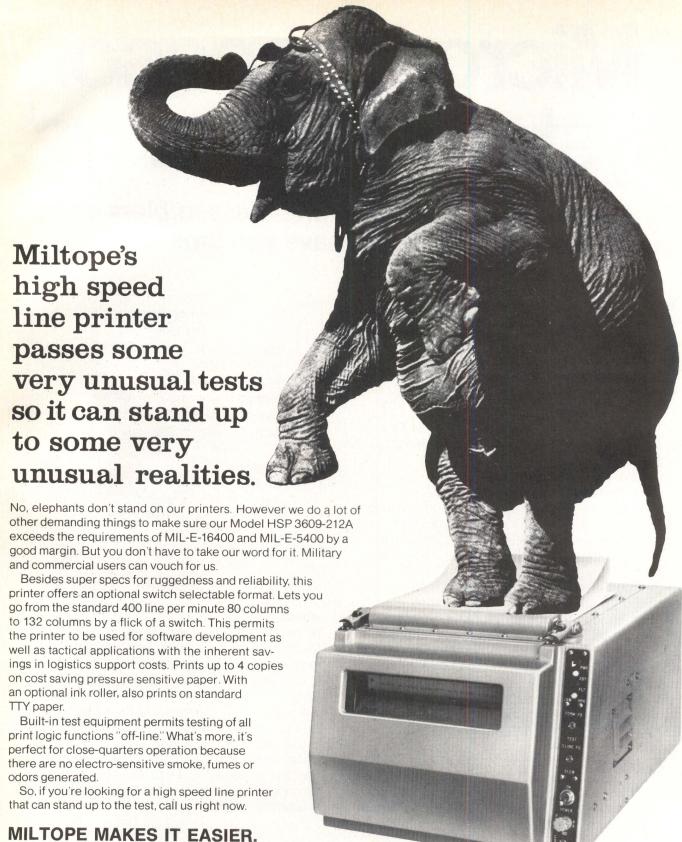
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APPLICATION NOTE

Designer's Guide For Selecting Magnetic Mini-Media

A. Bruce Manildi

Information Terminals Corporation Sunnyvale, California

Magnetic mini-media products have paralleled the growth of LSI chips in higher capabilities, wider applications, and lower costs. This guide matches mini-media performance against price for designer evaluation

The introduction of magnetic minimedia products parallels the growth of large-scale integration circuit chips. Until about four years ago, the only mini-media products widely used were the Philips cassette and the magnetic card. Then the 1/4-in (0.635-cm) data cartridge was introduced, followed in rapid succession by the diskette, mini data cassette, mini data cartridge, and Minidiskette.* Just as with semiconductors, magnetic media proliferation has led to a wider choice of solutions for the equipment designer, and a better match to specific applications. In the case of magnetic storage systems, the designer can choose a magnetic medium which more clearly meets requirements for storage capacity, access time, transfer data rate, and cost.

Cassette

As the most mature of the magnetic mini-media, the cassette is the most widely used. Its capabilities and liabilities are well known to system designers; therefore, most storage systems that use digital cassettes today are very reliable and well suited to the application.

Cassette drives, with their relatively small size and low power requirements, are highly adaptable for remote data collection. They are also used as storage systems (archival) on low cost minicomputers and for data file storage on many small busisystems. Typically, cassette drives use dc motors that can be accelerated rapidly, resulting in low power requirements and nearly zero standby power. However, in order to gain accurate control of tension and speed in the cassette, as many as three or four motors are necessary along with their attendant sensors; thus, the cost of high precision cassette drives can be high.

Primary functions of cassettes are data storage, data protection, and tape path control. More than 0.5M bytes of data can be stored in serial fashion at reliable, relatively low densities. Head-to-tape contact is assured through the use of appropriate pressure pad configurations.

Cassettes should be kept in a proper container between use, such as in the package supplied with the cassette. As with other storage media, the magnetic tape is susceptible to damage and contamination through the openings in the cassette. In addition, the cassettes should be placed away from the strong magnetic fields, and extremely hot temperatures must be avoided. If exposed to extreme environments, the cassette should be stabilized at room temperature before data recovery is attempted. With careful use, the life of a cassette can be between 2k and 20k passes, with no increase in error rate.

^{*}Minidiskette is a registered trademark of Shugart Associates, Santa Clara, Calif.

Cost, Speed, and Capacity Comparison of Low Cost Magnetic Recording Media Vs Paper Media

Media Type	Cents/Byte*	Typical Unit Capacities (Bytes)	Typical Transfer Rates (Bytes/s)	Average†† Access Times (s)
Typing Paper (One page, single-spaced)	0.0005	2000	15	60
Punched Card (80 columns at 600 cards/min)	0.0010	80	800	150**
Punched Paper Tape (1000 ft, 304.8 cm, reel or Z-fold)	0.0030	120,000	30 to 120	500
Magnetic Card	0.0080	5000	200	10
Cassette (Incremental, 290 ft, 88.4 cm)	0.0021	360,000	3600	20 to 100
Cassette (Blocked, 290 ft, 88.4 cm)	0.0014	540,000	3600	20 to 100
Minicassette (Blocked, 50 ft, 15.2 cm)	0.0060	64,000	200	320 to 150
Diskette (77 tracks, one side)				
(Flippy,† two sides)	0.0020	240,000	31,250	0.45
	0.0014	480,000	31,250	0.45
1/4-In Cartridge (Blocked, 300 ft, 91.4 cm)	0.0009	2,160,000	6000	20 to 60
Minicartridge (Blocked, 150 ft, 45.7 cm, two tracks) Minidiskette	0.0055	270,000	4000	15
(35 tracks, one side)	0.0041	109,000	15,625	0.8

††One-half of the maximum time required to recover any byte of data

Minicassette

Minicassettes build on and extend the strengths of standard cassettes. Reduced size implies a very small, low power drive, on the order of two times the size of a cigarette pack, with an operating power of approximately 0.75 W and nearly zero standby power. With low power, small size, and light weight, minicassettes are ideal for remote or portable battery-powered applications. They are also well suited to the personal and home computer market, due to their low cost and relatively low data transfer rate. Whereas standard cassette drives use up to four motors, most

minicassette drives use a single motor, although two motors are used in some designs. Digital minicassettes include write protect and end-of-tape detection capabilities.

Drives can be purchased in quantity for \$75 each, while the minicassette itself carries the lowest price tag per package of any mini-media. It should be noted that audio minicassettes are physically incompatible with digital minicassettes and will not fit in digital drives.

Diskette

Random-access capability is the strongest attribute of the diskette. The

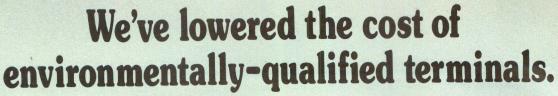
storage system, and therefore the user, can access any piece of data on the disc in less than one-half of a second. The amount of data varies from 0.25M bytes to over 1M bytes for double-density, double-sided versions. Diskette data rates are higher than for cassettes-between 250k and 500k bits/s—and more closely match system rates.

Although the diskette occupies little volume (0.5 in³, 8.2 cm³) and is easy to store and mail, the drive is relatively large (two to five times the size of a cassette drive), and consumes upwards of 60 W of operating power, with a minimum of 30 W in standby.

^{*}Byte = 8 bits

**Selecting one character out of 3000 cards

†Flippy is a registered trademark of Information Terminals Corp, Sunnyvale, Calif





Cost of a diskette drive is approximately \$400 in quantity. In the past, controllers and interfaces for diskette drives were considerably larger and more expensive than those for longitudinally recorded media. However, recent advances in semiconductor technology have resulted in a generation of "smart" controllers, consisting of a handful of large-scale integration (LSI) chips, and costing no more than a cassette or cartridge controller. Applications for diskettes began with data entry to replace punched cards, but have grown to include uses such as system discs on minicomputers and working storage devices for word processors.

The diskette's soft jacket must be treated carefully so as not to damage the medium within. The disc should be returned to its protective envelope when not in use, in order to protect the magnetic head access opening. Placing heavy objects or coffee cups on the disc or writing on the label with a ballpoint pen should be avoided; a felt-tipped pen should be used.

Minidiskette

As the minicassette was built on the strengths of the cassette, so the Minidiskette was built on proven diskette technology. This device, with its small size and random-access capability, is compatible with the fast growing word processing and programmable calculator market. Storage capacity is about 20 typewritten pages or just over 100k bytes of digital data. Average access time is on the order of 1 s, and data rate is exactly half that of the large disc at 125k bits/s.

The Minidiskette is a scaled-down, 5½" (13.34-cm) square version of the standard diskette. However, the associated drive is less than one-fifth the volume of that for the larger diskette drive. To overcome the liability of high power in the larger drive, the Minidiskette uses a dc drive motor and only consumes 15 W running and 7.5 W in standby.

Another significant advantage of the Minidiskette is its cost, about twothirds the price of the standard diskette. The drive sells for approximately \$200 in large quantities. Therefore, this storage device is highly attractive to low cost markets, such as personal or home computer use.

1/4-inch Data Cartridge

Although the ½-in (0.635-cm) data cartridge appeared on the market before the diskette, its impact has not been felt until recently. This data cartridge offers four times the storage capacity of the cassette since it has four tracks instead of two and writes at twice the density, 3200 flux transitions/in (ftpi) instead of 1600 ftpi.

By completely enclosing the tape in the cartridge when it is not inserted in the drive, most of the vulnerability relating to externally generated debris is eliminated. This is accomplished through the use of a driveactuated head-access door and a single-point drive. This arrangement reduces cost and complexity of the drive and eliminates the access holes for reel motors, capstans, and pinch rollers. Access holes necessary for detecting beginning-of-tape (BOT), load point (LP), early warning point (EW), and end-of-tape (EOT) have been eliminated through use of a transparent cover and a mirror situated at a 45-degree angle to and behind the tape path.

A single, simple servo is required for the motor. This servo controls speed and acceleration of an isolastic belt which in turn drives the magnetic tape and controls its tension. Additional reel motors are not needed. Since the tape handling elements of the drive are integral parts, cost of the cartridge is, as expected, higher than that of other magnetic minimedia products.

Even though the cartridge is relatively immune to handling damage, it should not be exposed to high temperatures or rapid temperature changes. After such exposure, or after extended periods of storage, it is recommended that the cartridge be operated through a tensioning pass from BOT to EOT to BOT before attempting data recovery.

Minicartridge

The minicartridge has the same configuration as that of the large cartridge and uses the same isolastic belt drive technique. A strong attribute of

the minicartridge is its relatively small size, about the same as that of a standard cassette. The very small and simple drive, with a single drive motor, is low in cost, nearly as inexpensive as the minicassette drive; however, the minicartridge cost approaches that of the large cartridge. An additional attribute is packaging. As in the large cartridge, packaging implies reliability and high system performance; it is a sturdy, well-built, compact data storage device.

Data storage capacity of the minicartridge is one-half that of the standard cassette as it utilizes cassette tape (0.150 in, 0.381 cm wide) with two tracks and the same density, but only 140 ft (42.67 m) of tape instead of 300 ft (91.44 m). In addition, unit cost is approximately twice that of the cassette. Therefore, cost per byte is considerably higher than that of the cassette.

In applications where drive cost is paramount, low equipment cost is important, or ratio of number of cartridges to drives is low, the high cost of this media is less forbidding.

Summary

Each magnetic storage device has individual positive and negative characteristics. It is the designer's responsibility to determine the minimedium best suited to the application. One characteristic which is often compared for all types of media is cost per byte. Even though this comparison can be made from the statistics in the Table, the system designer must be careful to note that these costs only apply to the case where the medium is completely used within the format requirements.

For example, a particular application may only require 64k bytes maximum. If this application were to use a minicassette, the cost would be 0.006 cent/byte; if a ½-in cartridge were used, the cost would be 0.03 cent/byte [((2.16 x 10⁶ bytes) ÷ (64 x 10³ bytes)) x 0.0009 cent/byte]. All magnetic configurations discussed here (except magnetic cards) would be capable of satisfying these requirements. Note that the cost per byte would be highest, not lowest, for the ½-in data cartridge.



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In the future, the cost per byte for diskettes will decrease due to increasing densities and the use of both sides of the media. But this cost decrease is only potential, since the application must be able to utilize the extra capability.

While radically different magnetic mini-media configurations are not foreseen for the immediate future, increased storage capacities will be emphasized. For example, a new cassette application stores 360M bits on eight tracks. Diskette systems having heads on both sides of the disc and double-density encoding are now appearing. There are cartridge applications that increase both linear density on the media and data density through coding schemes. Storage capacity in the 1/4-in data cartridge and minicassette will increase through increased tape lengths.

To benefit fully from increased data capacity, the user must undertake adequate training in media maintenance and use. Extreme caution must be exercised since tiny pieces of debris or minimal damage could cause data dropouts or errors. However, with proper treatment, magnetic mini-media products are reliable, low cost, effective solutions for data storage requirements.

Acknowledgement

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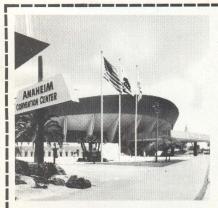
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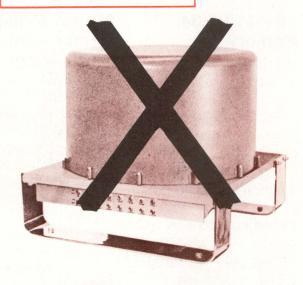


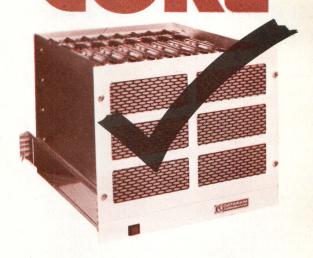
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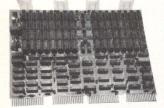
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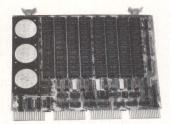
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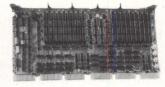
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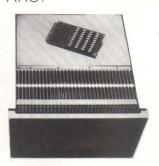
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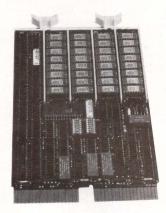
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Microcomputer Interfacing: Data Acquisition

Jonathan A. Titus Christopher Titus Peter R. Rony David G. Larsen

Tychon, Inc

Virginia Polytechnic Institute & State University

In the previous month's column, the software provided an example of a program used to acquire a single analog point in digital form. Since our general interest is in applications involving a series of points to be acquired, stored, displayed, and perhaps manipulated, this month's column will explore the use of microcomputers for data acquisition.

First, assume that the analog-to-digital converter (ADC) is interfaced as shown in last month's column. The software, repeated in Table 1, is also assumed to be the same. The digital value of the analog voltage is returned in the B and C register (register pair B).

In most data acquisition programs, a fixed number of points are to be acquired over a fixed period of time. In this instance, 100 points will be taken, one every second, and stored in read/write (R/W) memory for later use. In writing data acquisition software, three tasks must be performed in addition to the actual ADC task: a software counter to count 100 points, a 1-s timer, and software to store the data values must all be provided.

To count the 100 acquired points, the necessary software actually counts 100 passes through the data acquisition software. A general-purpose register within the 8080 chip is well suited for this; conditional jump instructions may be used to detect when the count is decremented to 0. While the counter may be either incremented or decremented, decrementing is probably easier for those who are just beginning to program

		TABLE	1		
Typical	Input	Routine	for a	10-Bit	ADC

	*100 000	
100 000 365 ADC,	PUSHPSW	/Save register A & flags
100 001 323	OUT	/Strobe the ADC to start a conversion
100 002 037	037	
100 003 333 TEST.	IN	/Input status bit and two MSBs
100 004 066	066	
100 005 306	ADI	/Add 1 to the flag bit
100 006 200	200	/to cause a carry if it is set
100 007 322	JNC	/No overflow, check it again
100 010 003	TEST	
100 011 100	0	
100 012 107	MOVBA	/Overflow, flag = 1, so save MSBs
100 013 333	IN	/Input the eight LSBs
100 014 065	065	
100 015 117	MOVCA	/Store them in register C
100 016 361	POPPSW	/Restore register A & flags
100 017 311	RET	Return to main program

TABLE 2
100-Point Data Acquisition Routine for 1 Point/s

		DW ADC 100 000	
		*070 000	
070 000 061	START,	LXISP	/Load the stack pointer
070 001 377		377	
070 002 070		070	
070 003 041		LXIH	/Load the data storage starting
		000	/address in registers H & L
070 004 000		072	7 address in registore in a 2
070 005 072			/Call the ADC software
070 006 315	CONVRT,	CALL	/shown in Table 1
070 007 000		ADC	/snown in Table I
070 010 100		0	
070 011 161		MOVMC	/Store the eight LSBs to memory
070 012 043		INXH	/Increment the memory pointer
070 013 160		MOVMB	/Store the two MSBs to memory
070 014 043		INXH	/Increment the pointer again
070 015 175		MOVAL	/Get the low address value
070 016 376		CPI	/Compare it to the 201st address
070 017 310		310	/310 = 200 decimal
070 020 312		JZ	/Done yet?
070 021 047		DONE	/Yes, jump to "done"
070 022 070		0	
070 022 070		CALL	/No, do the 1-s delay
		DELAY	7140, do the 1 5 dolay
070 024 031			
070 025 070		0	(After the delay not the payt
070 026 303		JMP	/After the delay, get the next
070 027 006		CONVRT	/ADC data point
070 030 070		0	
		/This is the 1-s time delay /subroutine	
070 031 365	DELAY,	PUSHPSW	/Save register A & flags
070 032 325	,	PUSHD	/Save registers D & E
070 033 021		LXID	/Load counter registers
070 033 021		000	
		110	
070 035 110	DEC	DCXD	/Decrement the register pair
070 036 033	DEC,		/ Decrement the register pun
070 037 172		MOVAD	
070 040 263		ORAE	W10 de la
070 041 302		JNZ	/If not 0, do it again
070 042 036		DEC	
070 043 070		0	
070 044 321		POPD	
070 045 361		POPPSW	
070 046 311		RET	
		/The program will cause /jump here when it has a /data points. A display or /might be placed here ins	cquired all the other routine
070 047 166	DONE,	HLT	



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alpha data

20750 Marilla Street, Chatsworth, CA 91311 TWX (910) 494-4914 microcomputers. Storing data in memory is not difficult. Once the converter value is stored in a register pair, the H and L registers (register pair H) may be used as memory pointers to point to a R/W memory location. Note that a complete 16-bit address must be specified for the MOV M,r instructions. Since data are acquired from a 10-bit ADC, two successive memory locations must be used to store each point. The INXH instruction (increment register pair H) provides an easy means of pointing to the next successive memory location. Data are stored by placing the eight least significant bits in location n and the two most significant bits in location n+1.

The 1-s timer may present some problems, depending upon the type of system used. It is relatively easy to write a 1-s software delay program using a series of register decrementing loops nested one within the other; however, this means that the computer must be doing nothing else in order to accurately time a 1-s period. In a system which is dedicated to data acquisition for the 100-s period, such a procedure is valid. If interrupts occur or if the computer cannot be allowed to "do nothing" most of the time, an alternate solution is needed. One possibility is to use an external clock, often called a real-time clock, which is unaffected by computer execution times, interrupts, or slow 1/0 devices. Once started, it continues to run at an accurate rate until it has timed the particular period of interest and sent an interrupt to the microcomputer. Some real-time clocks are free running, always keeping time. Others are programmable or preset for a particular period. The free-running clock interrupts the computer at repetitive intervals while the programmable clock interrupts the computer only once, at the end of its preprogrammed period. Integrated circuits such as the Intel 8253 and Texas Instruments TMS 5501 contain time-keeping circuitry that is easily interfaced to most 8080 systems.

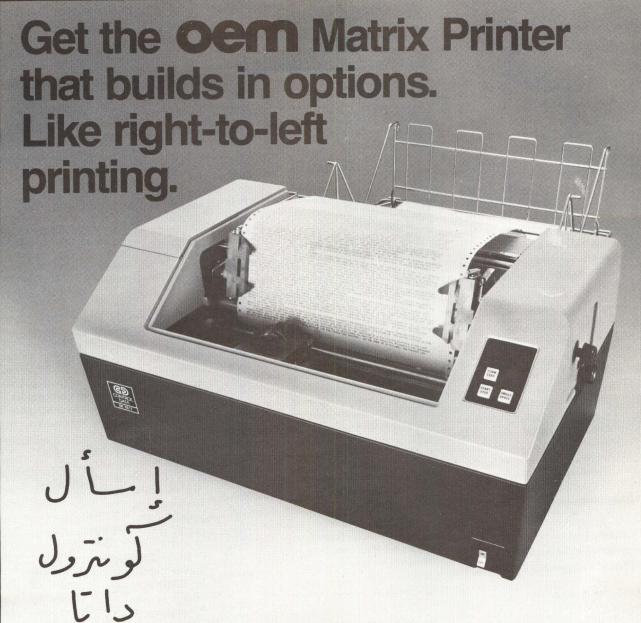
For simplicity, a software clock, rather than an interrupt-based real-time clock, will be used in this example. The software for the 100-point data acquisition program is shown in Table 2. After completing the program, the computer might be programmed to jump to the type of data display software discussed previously. The program does not contain a separate register to count the 100 passes through the data acquisition software. Since the memory address stored in registers H and L is already a counter, we have chosen to detect the 200th address rather than the 100th loop. This saves an internal register. Instead of decrementing a counter and detecting the 0 condition, the contents of register L are compared to the final address and the equality is used to signal the end of the loop.

and the equality is used to signal the end of the loop.

ADCS are not "instantaneous" devices which can perform a conversion in only a few microseconds. In many real situations, the analog input to the converter varies while the ADC is trying to perform a conversion, presenting the converter with a problem. How does it know what the real value of the voltage is? In most systems the ADC module has a sample-and-hold (SH) on the analog input. The SH circuitry samples the analog voltage when pulsed to provide a steady analog output to the ADC for conversion; the ADC is then pulsed to start the conversion. The Intersil IH 5110 is a typical sample-and-hold device.

This article is based, with permission, on a column appearing in American Laboratory magazine.





For a system house marketing to the mideast, Control Data adapted its Model 9317 Matrix Printer to print Arabic style:

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Three Plug-In Systems Expand Memories of Various Microcomputers

Memory capacities of the Motorola MEK6800D2 kit, DEC LSI-11, and Intel SBC 80/10 microcomputers have been expanded by the addition of three plug-in memory systems introduced by Motorola Integrated Circuits Div, 3501 Ed Bluestein Blvd, Austin, TX 78721. The MMS68104 memory card is a 16k x 8-bit system that is pinout compatible with the "D2" kit. The MMS1110 is a hardware- and software-compatible 16k x 16-bit system that plugs into the H9270 backplane slot of the LSI-11; 8k- and 12k-word versions are also available. Pin-compatible with the SBC 80/10, the MMS80810 is a 32k x 8-bit system, also available in 16kbyte versions.

For the three systems, max access times are, respectively, 650, 575, and 400 ns; and min read and write cycle times are 1.6 μ s, 750 ns, and 760 ns. Max active power requirements are 1.4 A, 16.8 W, and 13.6 W; standby is 1.1 A, 6.7 W, and 9.1 W, respectively.

Circle 170 on Inquiry Card

Software/Hardware Combination Offers Multitask Capability

Reducing both hardware cost and product development time, the 80D disc system and MUTE software package provide a multiuser, multitask disc operating system to users of microcomputer-based оем and development systems. MuPro, Inc, 424 Oakmead Pkwy, Sunnyvale, CA 94086 has developed the software to operate with the company's family of microcomputers, development systems, and in-circuit emulators. It supports BSAL-80 software consisting of the relocating block structured assembler, linking loader, and text editor.

Features include multiple terminal/multiple tasking capabilities for timesharing applications, with as many as 256 tasks divided into 64 priority levels; I/O support for many peripherals; comprehensive file management system; real-time clock which provides an accurate time reference; and error diagnostics. Through

the use of scheduling and interrupt processing algorithms, the system effectively manages execution and switching tasks. Due to reentrant coding, efficiency of BSAL-80 language, and use of overlays for seldomutilized routines, memory requirements are less than 16k bytes.

Additional characteristics of the software are availability of file utility routines to format, copy, and compress diskettes; concurrent interrupt-driven 1/0; and batch processing

capability.

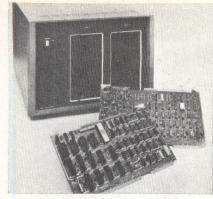
The 80D disc system hardware is compact, complementing the portability of the 80 microcomputer. A dual-spindle diskette drive mechanism utilizes voice coil head positioning techniques to provide an average seek time of less than 50 ms. The disc formats are soft-sectored, IBM 3740-compatible.

Requiring only a single circuit card position in the 80 chassis or OEM subassembly, the controller accommodates up to two dual drive units or four single drive units. Upper/lower head selection can provide twice the normal 256k bytes of available storage per diskette through double-sided recording. All data transfers between memory and disc are via direct memory access. Enclosed in a case measuring 4.6 x 10 x 21" (11.68 x 25.4 x 53.34 cm), the system also contains a software programmable real-time clock. Circle 171 on Inquiry Card

Double-Density Diskette Intelligent Controller Provides Greater Storage

A self-contained controller that handles up to 2M bytes of floppy disc mass storage serves the needs of users requiring more random-access bulk storage, without the costs of cartridge disc drives or magnetic tape. The OEM Computer Systems Group of Intel Corp's Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051 has introduced the SBC 202 double-density diskette controller which interfaces SBC 80 singleboard computers and System 80 packaged OEM computers with most types of double-density diskette drives, including the Shugart SA 800-1.

The controller operates on the company's Multibus[™] as an intelli-



Handling up to 2M bytes of floppy disc mass storage, Intel's controller for double-density diskettes is comprised of channel and interface boards. It contains a preprogrammed bipolar processor, enabling it to operate as an intelligent peripheral to SBC 80 singleboard and System 80 OEM computers

gent peripheral. Multiple computers can share mass storage resources and process concurrently. Multiple controllers can also be used on the bus.

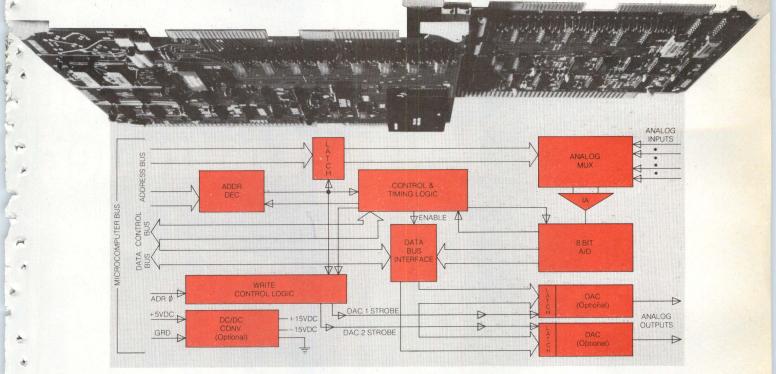
Two 6.75 x 12" (17.15 x 30.48-cm) boards comprise the unit—a channel board containing the 8-bit processor decodes commands, fetches parameters, and controls operations; and an interface board handles communications between drives and CPU, and implements all DMA and CRC. The DMA channel design enables processing of data in parallel with block transfers between diskette and computer memory. The processor operates with a 512-byte microprogram stored in Intel 3604 bipolar p/ROMS.

Recording occurs in a high density, soft-sectored format that allows up to 500k bytes to be stored on each diskette, and the controller can handle up to four drives for a full 2M bytes of total data storage. Track format is 52 sectors with 128 bytes/sector.

Simplified computer programming is achieved through preprogramming of the high speed processor (implemented with the company's series 3000 bipolar microcomputer set) to handle a set of high performance diskette operations upon receipt of an I/o command from the SBC 80. Operation parameters are specified by the computer, which prepares and stores 1/0 parameter blocks (seven bytes long) in memory, and gives the address of the block to the controller which refers to the block and implements the operation described. Single-unit price of \$1290 covers the controller supplied with a dual auxiliary connector, reference manual, and schematic.

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Burr-Brown announces the lowest cost Analog I/O Systems for Intel and Motorola microcomputers.



Prices start at \$198 in 100's. These new additions to Burr-Brown's growing family of Analog I/O Systems are designed specifically for Intel and Motorola microcomputer users. They're the only complete 8-bit systems available, and the lowest priced plug-compatible I/O systems offered for these microcomputers. Here's the complete hardware solution to your analog input and output interface problems. And it's a solution that simplifies system software too.

For the Intel SBC80 or Intellec * MDS user, our MP8600 series offers input and output on a single board which mates to either memory or I/O slots. These systems can provide up to 32 differential or 64 single-ended input channels. And they're adjustable from \pm 10 mV to \pm 5V full-scale to handle low or high-level signals directly. The two optional output channels have strap selectable full-scale outputs ranging from \pm 2.5V to \pm 10V.

Motorola Micromodule or EXORciser® users can choose the MP7400 series and get up to 24 differential or 48 single-ended input channels. Like the MP8600 series, input and output levels

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All of Burr-Brown's Analog I/O Systems (including our 12-bit systems previously introduced for Intel and Motorola microcomputers and our new 8-bit Pro-Log compatible systems) can be treated as memory by the CPU. New versions offer you the options of interfacing in the interrupt mode and of conversion without halting the CPU. This means essentially unlimited channel expansion capability plus easy software implementation.

These I/O interfaces are system engineered and specified to ensure compatibility with your microcomputer. That means big savings for you in development time, in system debugging and in production start-up.

If you're using a microcomputer from Intel, Motorola or Pro-Log, it will pay you to find out about Burr-Brown's 8 and 12-bit Analog I/O Systems.

For more information, contact Burr-Brown, International Airport Industrial Park, Tucson, Arizona 85734. Phone (602) 294-1431.

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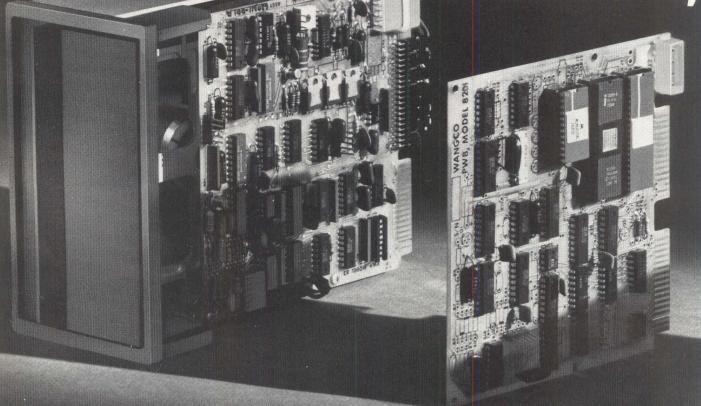
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LSI, the Wangco Micro-Controller is only 5½ inches square for easy mounting. The 8201 uses only 30 IC's in a low cost, reduced power, high reliability design, with nine macro commands including drive diagnostics, format and a data copy instruction. Up to four fives can be controlled by the 8201. A modified IBM-type soft sectored format is standard with optional double density available. The Wangco Micro-Controller interfaces easily with 6800 and 8080 microprocessors.

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The Wangco Microdiskettes[™] are certified for 40 tracks of data recording on both sides of the diskette. With double density encoding the total storage capacity on a single Microdiskette can be as high as 498.8 Kbytes.

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Two Versions of Software Accommodate Timesharing Applications

Altair Timesharing BASIC and Disc BASIC are magnified versions of the Extended BASIC, each with increased capabilities to accommodate up to eight different programs running simultaneously and independently within the system. Both versions run on the Altair 8800 series mainframe and CPU, with a minimum of 32k RAM, vector interrupt/real-time clock board, up to four 2SIO boards to interface terminals, and a line printer (optional for Disc BASIC). Disc BASIC also requires an Altair floppy disc drive and 88-p/ROM board. Various applications of the systems from MITS, 2450 Alamo SE, Albuquerque, NM 87106 include educational, scientific, and engineering uses.

Input and output are interrupt driven and fully buffered to provide instantaneous keyboard response. Operating with high speed, systematic job rotation, the CPU gives each job a 100-ms slice of the program. As a fixed partition system, each job is confined to a specific area of memory to prevent alteration or destruction. Memory areas can be different sizes.

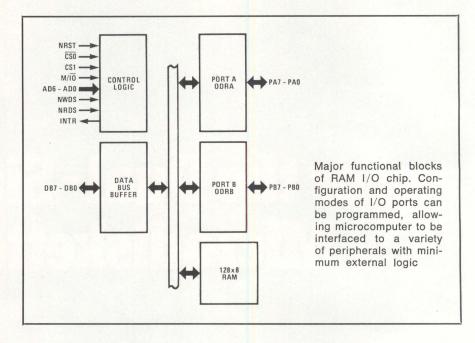
Timesharing Disc Basic facilitates listing of programs on a line printer, and provides rapid loading and program retrieval from the floppy disc. Timesharing Basic can be loaded from paper tape or audio cassette, with programs stored on paper tape.

Additional features include flexible 1/0 device support, extensive diagnostics for debugging, automatic line numbering, and line-oriented text editor with line and character manipulation capabilities. Control of a job may be transferred from one terminal to another with a single command; various control characters allow suspension and resumption of each job without data loss.

Circle 173 on Inquiry Card

Device Gives Independent Operation of RAM and I/O for Microcomputers

The RAM input/output chip (ISP-8A/650) is an LSI device which provides data storage and peripheral interfacing for microcomputer systems.



Developed by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, the device provides direct interface with the SC/MP-II.

The RAM portion contains 1024 bits of static RAM organized as 128 x 8. The I/O portion consists of two Tri-State^R peripheral ports of eight bits each. Each of the I/O pins in the two ports may be defined as input or output for maximum flexibility.

Ports may be read from or written to in a parallel (8-bit byte) mode. To improve efficiency and simplify programming in control-based applications, a single bit of 1/0 in either port is set, cleared, or read with a single microprocessor instruction.

In addition to basic I/O, one of the ports (A) may be programmed to operate in several types of strobed mode with handshake. This mode together with optional interrupt operation permits both high speed parallel data transfers and interface to many peripherals with no external logic.

Added features include low power dissipation and fully static operation. The chip is an n-channel silicon gate device packaged in a 40-pin DIP; it operates with a single 5-V power supply and is fully TTL compatible.

Universal System Tests and Debugs Prototype Microprocessor Products

In contrast to test equipment dedicated to specific microprocessor chips and limited primarily to software development, a Microprocessor Development Support System (MDSS) has been developed that interfaces directly with most microprocessor systems by means of "custom personality" boards containing appropriate circuitry and short compatible programs. The universal system that tests and debugs breadboards and prototype products is designed to

accommodate itself to the differences of diverse microprocessor systems.

Two types of instructions—monitoring and intercommunication commands—are provided. The system can be used interactively, with the operator monitoring and controlling the performance of the prototype in real time through an associated teleprinter or CRT terminal. Software can be monitored or altered and hardware problems detected and isolated.

When the prototype is hooked up by means of a flat cable, the operator can determine running conditions of the device under test, make software alterations, and re-execute the

HE REMARKABLE 3843 USART: IT HELPS

It also helps dumb peripherals speak fluent parallel. Quite possibly, our new 3843 is the best communications idea to come along since tin cans and string. Here are the details:

WHAT IN THE WORLD IS A USART?

The 3843 is a full duplex Universal Synchronous/ Asynchronous Receiver Transmitter (hence, USART) designed to interface the bus-oriented format of a controller with the serial format of peripherals.

It converts parallel data to formatted serial data and assembles formatted serial data for parallel use by the controller.

The new Fairchild device provides programmable control of the transmitting and receiving mode, character length, framing format, parity mode and baud rate. Inputs and outputs are TTL-compatible. Three-state outputs can be combined to form a TTL-compatible output bus.

A FEW MEANINGFUL SPECS.

The 3843 provides 5, 6, 7 or 8-bit selectable character length. Odd or even parity generation and checking. Selectable number of stop bits $(1, 1\frac{1}{2}, 2)$ in asynchronous mode. Selectable clock rates (16X, 32X, or 64X-baud rate). Maximum baud rates (synchronous mode): 1X clock, 256K; 16X clock, 16K; 32X clock, 8K; and 64X clock, 4K. Error flags include over run, parity and framing error. Requires + 12V, +5V supply voltage.

On one low-cost programmable chip, requiring minimal power and pin-count, you get essentially all the functions necessary to interface a parallel data environment with a serial communications link. It is ideal for use with any 8-bit

> microcomputer system, including Fairchild's F8 and F6800 families.

The 3843 is manufactured with the N-channel Isoplanar™ silicon gate process. It's available in both plastic



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The new USART is the first device in a new line of telecommunications products from Fairchild. The 3843 is available right now, in quantity. Call your Fairchild distributor, sales office

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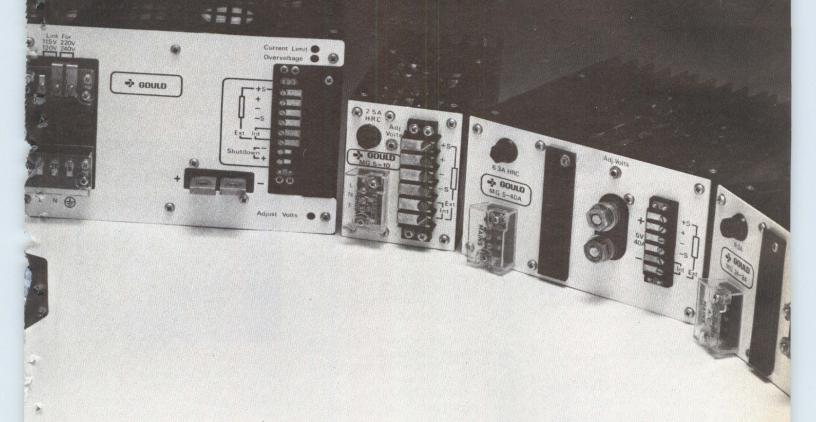
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company like Gould could offer. For after sales service Gould warranty repair centers are located worldwide.

For complete specifications on our entire switcher line or to arrange for a free evaluation unit, contact Gould, Inc., Power Supply Division, 4601 North Arden Drive, El Monte, CA. 91731, Telephone (213) 442-7755. Gould. The power in switching power supplies.



CIRCLE 65 ON INQUIRY CARD

modified program. By entering the assembled program into RAM rather than p/ROM, immediate corrections can be made to data or program steps. Software features include trace, freeze, and step commands.

Applications involve development of software for different microprocessors, performance of typical logic analyzer functions, and differentiation between hardware and software faults during prototype debugging. Operating with microprocessor-based subsystems of any description, the system is insensitive to the type of product being tested. Personality board interfaces include those for the Intel 8080, National Semiconductor PACE, and Motorola MC6800 series; they will be extended to cover additional microprocessors in the future.

Arthur D. Little, Inc, 25 Acorn Pk, Cambridge, MA 02140, which originally designed and built the instrument for its own purpose, has made it available to clients as a wired-up, standard package in the \$10,000 price range. The consulting firm is seeking a manufacturer to commercialize the design on a high volume basis.

Communications Interface Combines USART and Baud Rate Generator Functions

A cost-effective solution to many data communications problems has been found in the 2651 programmable communications interface (PCI), which is a MOS/LSI circuit combining the functions of a USART with those of a baud rate generator in a single 28-pin DIP. According to Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, it is the first such unit designed for 8-bit microprocessor serial communications.

Capabilities include modem control, support of IBM's BiSync protocol, asynchronous echo mode, and local and remote self-testing. The fully TTL-compatible chip operates from a single 5-V supply, and requires no system clock. Internal baud rate generator provides 16 program-selectable rates for the transmit and receive clocks; external baud rates may also be selected.

Double-buffered transmitter and receiver sections permit either halfor full-duplex operation. The PCI serializes data characters from the microprocessor for transmission, and assembles an incoming bit stream into parallel characters for input to the microprocessor. It is programmed to handle characters from five to eight bits in length.

Circle 175 on Inquiry Card

DMA Multiplexer Expands LSI-11 Up to 128 Channels

The increase in available processing power coupled with the ability to expand to 128 ports, obtained from the Mighty-Mux 11L direct memory access multiplexer, serves to enhance the DEC LSI-11. The complete 1/o system uses DMA rather than individual character handling to reduce 1/o processing overhead from over 70% to less than 2%. This, together with the availability of four status and control lines on each port, enables the computer to interface with up to 128 local peripherals or remote devices equipped with serial interfaces.

All important parameters are under program control on a port-by-port basis. The program also controls parity mode, character size, automatic echo, and baud rates for each port. Asynchronous or synchronous operation is selectable.

Standard features of the system from Educational Data Systems, Inc, 1682 Langley Ave, Irvine, CA 92714 include interfacing to EIA RS-232-C or RS-422, or current loop; and half-or full-duplex operation. The device is priced at \$1600 for the basic 4-port module; expansion is in 4-port increments up to 128. Support software and equipment are available. Circle 176 on Inquiry Card

Software Package Combines BASIC With Compiler Technology

Reductions in time and cost of software development is achieved with the powerful high level Dynabasic^R software development system for the company's M6800-based microcomputer and floppy disc system. Compiler technology is combined with BASIC in this package which produces efficient object code approaching that

of programs coded in assembler. The package is suited to both OEMS and end users.

Two configurations of the system are available from Dynalogic Corp Ltd, 141 Bentley Ave, Ottawa K2E 6T7 Canada. The full development system, which sells for \$750, has all features necessary for efficient program development. It requires a minimum of 24k bytes of RAM. Once operational, the program can be run under a compatible runtime system requiring only 8k bytes of RAM. It costs \$250. The package is fully compatible with the company's DYNAMO operating system.

Circle 177 on Inquiry Card

40-Col Alphanumeric Printer Accepts Data Directly From µComputers

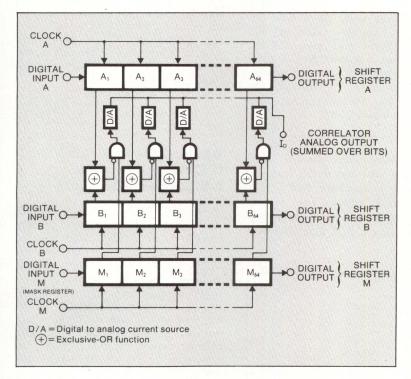


With either 8-bit parallel or serial interfaces, the AIP-40 standalone tabletop printer for microcomputer development systems, terminals, and data acquisition TTY printer replacement can print up to 40 columns on adding machine roll paper using a 5 x 7 dot matrix impact printer. Up to 64 8-bit ASCII-coded letters, numbers, and special characters are accepted directly from the PIA circuits offered with 8080, 6800, and other microprocessors, and are printed at a rate of 50 char/s. Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 is offering the device with housing, print mechanism, and choice of ac power supply and interface electronics, starting from \$425 in single units. A serial ASCII TTY/RS-232-C 2-wire option is available. Circle 178 on Inquiry Card

65-Line/Min Capability of Impact Printer Enhances M6800 Systems

For use with M6800 development systems, the EXORprinter connects

Revolutionary NEW 64-bit 15 MHz Digital Correlator.



TDC-1004J

Features:

- 15 MHz correlator speed
- 30 MHz shift speed (static shift registers)
- Analog current output, proportional to degree of correlation between registers
- Mask register: Used to select "Don't Care" (no effect on correlation) bit positions if desired
- Monolithic, bipolar TTL
- 16 pin C DIP
- 0-70°C operation
- 200 mW power consumption
- Only \$150 each in 100's

Applications:

- Image comparison/recognition
- Bit/word synchronization
- Bit/word detection
- Error correction coding
- Pulse compression
- One's or zero's counter

The TRW TDC-1004J is a 64-bit digital correlator capable of operating at 15 MHz with analog correlation output. Digital parallel correlation is a signal processing technique used for bit synchronization, bit detection, error correction coding, pulse compression and other applications. Correlation takes place when two binary words are serially shifted into two independently clocked shift registers. The two words are continually compared bit-for-bit by exclusive-OR circuits.

Each exclusive-OR circuit controls a current source D/A. The current outputs of the D/A circuits are summed to produce the correlation function.

0

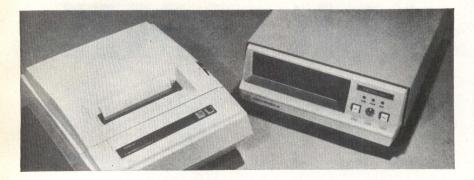
The mask register allows the user to selectively choose "no-compare" bit positions.

For detailed data, applications information and prices, contact your local TRW components sales office or call (213) 535-1831 or write TRW LSI Products, An Electronics Components Division of TRW, Inc., One Space Park, Redondo Beach, Calif. 90278.



TRW LSI PRODUCTS

...from a company called TRW



directly to the bus of an EXORciser or Micromodule system through a peripheral interface module and interconnect cable. The printer produces lines of up to 80 5 x 7 dot matrix characters at a max rate of 110 char/s (approx 65 lines/min). Printing on an 8.5" (21.59-cm) wide roll of paper using a conventional teleprinter ribbon, the printhead moves uniformly in both directions.

Motorola Microsystems, PO Box 20924, Phoenix, AZ 85008 has also added optoelectronic sensing, and a stepper motor with silent line advancing and a slew rate of 400 lines/min. MDOS and EDOS EXORdisk™ operating systems provide drivers and commands for the device which is available in 110-Vac, 60-Hz or 230-Vac, 50-Hz versions.

Circle 179 on Inquiry Card

Slave Expandable System Programs and Emulates p/ROMs

An MPU-based programmer/emulator features slave expandability, op-

tional cassette data storage unit, multiformat load and dump features, built-in p/ROM simulator, and a powerful resident editor. The Smarty contains an RCA 8-bit CMOS microprocessor, 1k x 8 data RAM, 128-byte

SLAVE BUFFERS

PROGRAMMER
2704/2708

DISPLAY

DATA
BUS

TO SLAVES

KEYBOARD

CASSETTE I/O

UART

TTY I/O

DATA RAM

PROGRAM
MEMORY

DATA RAM

ADDRESS
BUFFERS

HOST
SYSTEM

ADDRESS
BUFFERS

With permanently connected slaves for reliability and ease of use, Smarty p/ROM programmer/emulator from Sunrise Electronics has nearly all components mounted on PC boardonly fuse and power switch are wired in. For industrial, engineering, production, and quality control applications, device compares programmed p/ROM or ROM against standard to verify proper data, and programs large quantities of p/ROMs in minimum time by adding several slaves of the same type

scratchpad, display, and indicators. System software includes fault-tolerant I/O subroutines for BPNF, hexadecimal, packed binary, ASCII/HEX, or user defined format.

Once p/ROM data are loaded into the data RAM, the user plugs the emulator cable into the p/ROM socket of the microprocessor system to try the program. This system accesses the data RAM as if it were a p/ROM or ROM. Following editing, the user invokes the programming mode; programming is then done automatically. Data can be dumped onto punched paper tape, cassette, disc, or other media.

The system has sockets for 4k bytes of program memory of which 1k is used in the basic machine. As slaves, peripherals, or more powerful editing packages are added, Sunrise Electronics, 228 N El Molino Ave, Pasadena, CA 91101 will supply p/ROMS with programs to operate these features.

Circle 180 on Inquiry Card

Analog Input System Is Compatible With 8-Bit Microprocessors

A complete 16-channel data acquisition system designed to interface directly to 6800, 650X, and F8 type microprocessors is the self-contained MP21 hybrid, quad-in-line package. It houses a 16-channel analog multiplexer that accepts up to 16 single-ended or eight differential signals as well as interface, timing, and address decoding logic; high gain instrumentation amplifier; 8-bit A-D converter; plus all necessary address, data, and control bus interfaces.

Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734 has designed the system to be both timing and logic level compatible with the three microprocessors; thus no external logic is needed. Gain and offset are internally laser trimmed, eliminating external adjustments while providing absolute accuracy better than ±0.4% (1 LSB) on high level ranges.

Low level signals such as thermocouple outputs can also be handled directly with reduced accuracy. The instrumentation amplifier can be programmed with a single external resistor to provide input signal ranges as low as ± 10 mV rs. Additional features include delay timing and in-

put overvoltage protection.

NOW, LEARSEGLER AND BURROUGHS AREON SPEAKING TERMS.

You're probably very happy with your Burroughs mainframe.

But you'd undoubtedly like to have the versatility and dependability of Lear Siegler terminals. If only they were compatible with your present system.

Now they are. Complete with standard Burroughs polling and address line disciplines.

What's more, the ADM-2B's forms mode capability is compatible with the TD-820.

The ADM-2B gives you full text editing capabilities. Including erase to end of line/field/page. Insert and delete character and line. Blinking and blanking fields. And tabbing.

Just flick a switch and you can convert the ADM-2B to a standard ADM-2 with Burroughs line discipline.

Line diagnostic mode is switch selectable - which makes it extremely valuable for troubleshooting.

Of course, there's all the support that Lear Siegler is famous for. Throughout the United States and in many foreign countries.

\$2485

That's the full price. Including serial printer port. Numeric keypad. 24x80 character screen. 16 function keys. 110-9600 baud. RS232 interface. Burroughs two-wire direct connect is available as an option.

The fact is, Lear Siegler's new ADM-2B terminal gives you the best of both terminals. So you can use it right alongside your present Burroughs terminals and mainframe.

So rest easy, Burroughs users. Because now Lear Siegler speaks

your language.

For more information contact: Lear Siegler, Inc., E.I.D./Data Products, 714 N. Brookhurst St., Anaheim, CA 92803; (800) 854-3805. In California (714) 774-1010.



ADM-2B. ART TERMINAL



MICROPROCESSO

BOSTON October 17-21 NEW YORK October 24-28 DALLAS November 7-11 PHILADELPHIA November 14-18

TORONTO November 28-

Similar courses being offered in EUROPE. Write or Call: Integrated Computer Systems, Inc. Boulevard Louis Schmidt 84, Bte 6 1040 Brussels, Belgium Telephone: (02) 735 60 03 Telex: 62473 3 or 4 Day Engineer

2 Day Project Management Series

COURSE 111: One Day-MONDAY

Microprocessor Project Management

From design through manufacture, QA and field service

MICROPROCESSORS: HOW CAN YOU GO WRONG??? WHAT ABOUT...?

Underestimating software costs and time? Inadequate software documentation? Selecting the wrong microprocessor? Software development equipment(\$14000!)? Manufacturing problems? Hardware/software testing? Reliability? Obsolescence? . . .

A microprocessor project is different from anything you've managed before. This one efficient day of organized, expert guidance will save you literally months of wasted time, re-invented wheels, and costly oversights.

This unique course synthesizes the experience of hundreds of project managers (who learned the hard way) into a practical field-proven methodology for managing all phases of a microprocessor application. The course emphasizes high-risk, high-cost and time-critical problems unique to microprocessors. Concrete real-world case studies illustrate the methods presented, and these step-by-step methods can be immediately applied to your own project.

This course will benefit every manager and engineer concerned with microprocessors. Teams from engineering, manufacturing, QA, and field service are encouraged to attend (team discounts available).

KEY TOPICS

- 1. Fundamental concepts, definitions and jargon.
- 2. Avoiding pitfalls and "technical tunnel-vision."
- 3. Planning and specifying the project the PERT/flowchart.
- 4. How to select personnel and evaluate performance.
- 5. How to select the right microprocessor what's really important?
- 6. Software development and test equipment what's really needed?
- 7. How to estimate overall project costs and schedule.
- 8. How to manage software design and development.
- 9. Software documentation a practical methodology.
- 10. Verifying that the software works.
- 11. Manufacturing, testing and QA both software and hardware.
- 12. Component & product reliability planning μP field service.
- 13. How to prepare for the future today . . . and avoid obsolescence tomorrow.

SPECIAL LATE-AFTERNOON WORKSHOP

A unique opportunity to discuss your application-oriented problems in a productive shirtsleeves atmosphere. Immediately after Course 111 from 4:30 until 6:00pm with snacks and refreshments.

COURSE 102s: One Day-TUESDAY

Microprocessors and Microcomputers:

A Comprehensive Technical Introduction and Survey

This course provides a comprehensive unbiased introduction to microcomputer hardware/software development and integration. The course emphasizes the factors affecting key design and development decisions including: processor selection, I/O and software design, software implementation steps, development and test equipment, and most important pitfalls to be avoided when getting started. Throughout the course, applications examples provide concrete illustrations of concepts presented and are drawn from the following application areas: military, communications, consumer, instrumentation, industrial control, and biomedical systems.

This course is *vital* (1) to all engineers and managers who want a quick, unbiased, cost-effective introduction to microprocessors (2) to those engineers attending this as the first day of the "Engineering Design" series (Course 102s, 125A and 136) and (3) to managers attending this course as the second day of "Project Management" series (Course 111 and 102s).

COURSE OUTLINE

- 1. INTRODUCTION
 - What is a microprocessor (µp)? a microcomputer (µc)? Identifying suitable and unsuitable applications
- 2. FUNDAMENTAL MICROCOMPUTER CONCEPTS
 - Terminology Software (SW) how it works; how it's developed
 - Hardware (HW) Basic μc configurations
 The μc design cycle
- 3. THE HARDWARE
 - μp architectures (4, 8, 16-Bit and slices)
 Memory systems design ROM, PROM, RAM, CORE
 Input/output organization (programmable I/O, interrupts, DMA)
 Build or buy?
- 4. INTERFACING TO THE EXTERNAL WORLD
 - I/O port design Programmable LSI I/O chips Interfacing to: analog devices, keyboards, displays, cassettes, etc.
- 5. SOFTWARE DESIGN & IMPLEMENTATION
 - Four implementation methods Editors, assemblers, compilers
 - Assembly vs. high level languages (FORTRAN, BASIC, PL/M)
- 6. INTEGRATING AND TESTING THE HW AND SW

 What really useful tools are available? What tools should you build yourself? Isolating and fixing HW and SW bugs
- 7. TECHNICAL SURVEY OF μP'S AND μC'S
- Intel, Fairchild, Motorola, National, Rockwell, Signetics, Texas Instruments, Zilog, and others including the new LSI minicomputers
 Board-level μc systems — PROLOG, PCS, CONTROL LOGIC, WARNER/SWASEY, and others
- A systematic, application-oriented approach to selecting the right microprocessor family.
- 8. UTILIZING DEVELOPMENT AND TEST EQUIPMENT

 Logic analyzers SW simulators Specialized µc debugging equipment µc development systems Peripherals to buy
- 9. HOW TO GET STARTED
 - What equipment to buy first Pitfalls to avoid Good information sources

R EDUCATION

ec2

CHICAGO December 5-9 WASHINGTON, D.C. December 12-16

g Design Series

COURSE 125A: Two Days - WEDNESDAY & THURSDAY

Hands-On Microcomputer
Programming Workshop

Programming Workshop (for the beginner)

LEARN-BY-DOING
EACH STUDENT
RECEIVES A
COMPLETE 8080
MICROCOMPUTER
SYSTEM FOR HIS
PERSONAL USE
THROUGHOUT
THE COURSE.



This highly efficient, intensive short-course combines expert teachers and detailed course materials with unique opportunity to learn by immediately implementing on your personal microcomputer each new programming concept as it is developed by the instructor.

COURSE OUTLINE [with exercises in brackets]

- 1. INTRODUCTION TO THE ICS 8080 μC TRAINING SYSTEM

 Hardware configuration How to use the keyboard/display and built in commands [I] pading and executing a simple program]
- built-in commands [Loading and executing a simple program]
 2. SOFTWARE FUNDAMENTALS AND BASIC TECHNIQUES
 CPU Register Instructions [Counting] Memory Instructions
 [Storing & Retrieving Data] Basic I/O [Controlling LED segments] Jumps and Loops [Time delay program] Bit Testing
 [Binary Decoding] Subroutines & Stacks [Keyboard Input]

B. ADVANCED PROGRAMMING TECHNIQUES

Arithmetic [A multi-precision calculator]
 Data Organization
 [Table Look-up]
 Block I/O Transfers [Real-Time I/O]
 Controller Programs [Traffic Control]

4. PROGRAM DESIGN METHODOLOGY

 Systems analysis • Specifying the program • Design approaches (top-down, structured programming, modular design)

OPTIONS FOR POST-COURSE SELF-STUDY

Course 125B: Includes 125A PLUS attendee receives a microcomputer & a 650-page Self-Study Text to take home. Course 125C: Includes 125A PLUS microcomputer to take home.

COURSE 136: One Day - FRIDAY

Shop NEW! NEW!

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Hands-On Interfacing Workshop
(Limited to current or former attendees of Course 125.)

Utilizing the ICS training microcomputers and additional Interfacing hardware, students will learn both software and hardware for interfacing to the real-world.

In-Class Projects include:

- 1. Real-Time Interrupt programming (w/Intel 8253 timer)
- 2. A/D Conversion A Digital Thermometer
- 3. DC Motor Control (Open and closed loop)
- 4. Other (student-option) Interfacing projects

COURSE ENROLLMENT FORM

COURSE HOURS

Orientation: 8:30-9:00am Course Lecture: 9:00am-4:30pm Special Events: 4:30-6:00pm

In addition to the extensive hands-on exercises of Course 125A and 136, informal microcomputer hardware activities are organized at every course for valuable hands-on experience.

COURSE FEE:

Management Series: (2 days: 111 + 102s)-\$390 3-day Design Series: (102s + 125A)-\$495* 4-day Design Series: (102s + 125A + 136)-\$595* Complete Series: (111 + 102s + 125A + 136)-\$695* Individual Courses: 111 or 102s or 136 -\$195; 125A-\$395*

*Option 125B—add \$445; Option 125C—add \$350
Course Fee Includes: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discounts: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

TO ENROLL:

Please fill out, detach and return coupon. A confirmation with complete course details will be forwarded to you.

MAIL TO: Integrate

Integrated Computer Systems, Inc.

4445 Overland Avenue

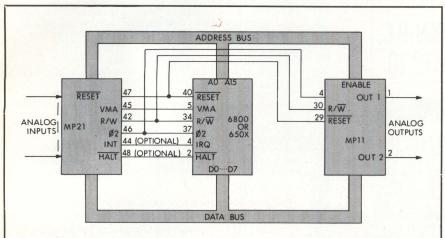
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For immediate confirmation, CALL:

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PLEASE ENROLL ME in the following Design Series					
courses: 2 Day Project Management Series					
COURSE	111	102s	125A	136	
BOSTON	Oct 17	Oct 18	Oct 19-20	Oct 21	
NEW YORK	Oct 24	Oct 25	Oct 26-27	Oct 28	
DALLAS	Nov 7	Nov 8	□ Nov 9-10	Nov 11	
PHILADELPHIA	Nov 14	Nov 15	Nov 16-17	Nov 18	
TORONTO	Nov 28	☐ Nov 29	Nov 30-Dec 1	Dec 2	
CHICAGO	Dec 5	Dec 6	Dec 7-8	Dec 9	
WASHINGTON, DC	Dec 12	Dec 13	Dec 14-15	Dec 16	
NAME JOB TITLE COMPANY MAILSTOP ADDRESS CITY STATE TELEPHONE () Ext PAYMENT: Please indicate method of payment. Check/M.O.enclosed P.O.included Please invoice me Please put me on your mailing list to receive future Course Schedules. Please send information on ICS Self-Study Courses. Please contact me with regard to On-Site Courses.					



Interconnections of Burr-Brown's analog input microperipheral with Motorola's 6800 or MOS Technology's 650X microprocessor are diagrammed. With different connection arrangement, Fairchild's F8 can also be used. Although device is optimized for 8-bit microprocessors, addition of a few external components enables it to be used with any 4- through 16-bit microprocessors

To simplify programming and allow for unlimited channel expansion, the unit is treated as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used to access data. Memory mapped operation allows the system to be used

with or without halting the CPU or in interrupt mode.

Housed in a 1.7 x 2.1 x 0.22" (4.3 x 5.3 x 0.56-cm) ceramic package, the 80-pin device has a temperature range of 0 to 70°C. Power requirements are 15 and 5 Vdc.

Circle 181 on Inquiry Card

Self-Contained µComputer Offers Expansion and Adaptability To Needs

A fully integrated, standalone system, the DE68DT microcomputer contains keyboard; 20-column alphanu-



DE68DT microcomputer is self-contained with integral tape drives, alphanumeric/numeric display and printer, keyboard, miniature floppy disc, and RS-232-C. Both desktop and compact portable models are available from Digital Electronics

meric display; 40-column impact printer; single or dual minicassette tape drives with up to 200k bytes/cassette; miniature floppy disc; RS-232-C ports for supporting CRT, printer, or modems; numeric keypad; and 9-slot card cage all fitted into the case with the 6800 CPU and power supplies. The system is an outgrowth of the DE68 previously announced by Digital Electronics Corp, 415 Peterson St, Oakland, CA 94601 (see Computer Design, "Micro Processor/Computer Data Stack," Nov 1976, pp 148, 150).

I/O capabilities include programmed, interrupt-initiated, and DMA data transfers. RAM expansion to 65k bytes, and 16k-byte EPROM cards are available options.

Software includes assembler, BASIC, and FORTRAN IV, as well as DEbug, a 6k-byte ROM/p/ROM operating system. A mnemonic translator permits software debugging in assembly language. Entry/display, search, and print modes are selectable, offering

assembly mnemonics, hexadecimal, or ASCII characters.

Applications are in instrument control, data acquisition and reduction, transaction logging, 6800 software development, and microprocessor education. Customization to user needs is achieved with a dual floppy disc drive or other peripherals which can be coupled to the 1/0 bus.

Two versions are the standard DE68DT desktop model weighing less than 30 lb (13.6 kg), depending on options; and the compact DE68C, without the miniature floppy disc, which weighs under 25 lb (11.34 kg). The portable units measure 22.25 x 17.5 x 7.5" (56.5 x 44.45 x 19.05 cm) and 19.5 x 20 x 5.5" (49.5 x 50.8 x 13.97 cm), respectively.

Flexible Series of Functional Cards Are Compatible With LSI-11s

A family of digital functional cards, offering optimum flexibility, is compatible with the DEC LSI-11 microcomputer series. The half quad boards measure 8.5 x 5" (21.59 x 12.7 cm). Adac Corp, 15 Cummings Pk, Woburn, MA 01801 is also offering an LSI-11 to Unibus translator and bus repeater.

Model 1616 and 1632 are TTL digital I/O cards with 16 or 32 I/O lines that can be field modified to be either inputs or outputs in increments of eight. The system can be configured in any combination of I/O lines with the use of pluggable components. With a 16-bit status register, the system can operate under either program control or program interrupt. All output lines are latched.

The digital input card that can detect contact closure on any or all of 16 discrete input lines is the model 1616-CCI. Status of lines, which is determined by a double read operation, is stored in a register and interfaced directly to the microcomputer bus; interface is in either program control or program interrupt mode. All inputs are debounced and latched.

Model 1616-HCO and 1632-HCO are digital output cards with 16 or 32 discrete latched outputs with high current capability to drive incandescent lamps. Plugging directly into the LSI-11 backplane, the driver contains bus transceivers, 16-bit status register, and flexible address scheme. It includes a program control interface and can drive loads up to 300 mA each returned to 35 V.

Intel delivers PDP-11 memory for people who can't afford to wait.

When you're in a hurry for more semiconductor memory for your PDP-11, call Intel. We deliver memory for the full PDP-11 line. And because we're the largest manufacturer of semiconductor memory in the world, delivery is when you want it.

Why wait? Since you've chosen the leader to supply your minicomputer, it makes sense to go to the leader for memory, too. That's us.

Intel memory systems save you more than time. Our in-1670 add-on memory for the PDP-11/70 is one example. It gives you four times the capacity in the same frame compared to the DEC MJ11-A core memory. And built in Error Correction Code (ECC) and Error Logging improve up-time and reduce maintenance time by automatically correcting and recording single-bit failures and detecting and recording double-bit errors.

For PDP-11 add-in memory go with our in-4711 plug in boards. You'll get memory that's even faster than DEC's. 16K words per hex-wide board. With or without parity. To further expand PDP-11 memory and reduce UNIBUS™ loading choose our in-4011 add-on. With memory management you can expand to 128K words in 16K increments. And since the in-4011 requires only one UNIBUS load, you get added system flexibility.

Get more memory for your LSI-11 and PDP-11/03 in less space with our in-1611 add-in memory. You get up to 32K words, in 8K increments, on a single, two-wide, board. That's up to eight times the memory you get with a DEC board.

When you can't afford to wait call us at 800-538-8476. In California and Canada, call 408-734-8102, x575. We'll save you time, and much more.

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	Days 🗆 30 Days 🗆 Days	I can't wait! Must have delivery in □ 5
	Ext	☐ Please call me at/
	semiconductor memory for the	☐ Please send me information on
	□ PDP-11/40	following:
	□ PDP-11/45	☐ LSI-11, PDP-11/03 ☐ PDP-11/04
	□ PDP-11/55	□ PDP-11/05
	□ PDP-11/70	□ PDP-11/34
		□ PDP-11/35
		Name/Title
on	Mail Station_	
		Address
		City/State/Zip_

CIRCLE 69 ON INQUIRY CARD

The last card of the series, model 1664 is a 64-line parallel TTL 1/0 card; all lines can be configured as either input or output lines, in increments of eight, by the use of pluggable components. A flexible address decoder is included. Communications with the four 16-bit registers is accomplished under program control.

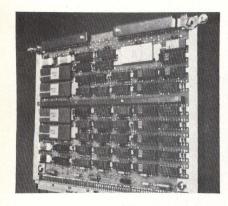
Claimed as the first bus translator to allow LSI-11 peripherals to operate with a Unibus CPU (any of the PDP-11 series), model 1900 can be inserted directly into the Unibus. The 8.5 x 10" (21.59 x 25.4-cm) board's major feature is that lower cost memories and peripherals that are available for the LSI-11 bus structure can be routed through the bus into the translator with integrated circuitry, making it compatible with the Unibus CPU.

The model 1950 bus repeater allows end users of the LSI-11 to employ a greater number of bus devices or longer cables than may be accommodated by the basic bus. Circuitry is contained on a half quad board. Several repeaters may be used in a system to daisy-chain card cages together. A cable set [up to 50 ft (15.24 m)] and cable terminator are also available.

Circle 183 on Inquiry Card

Militarized µComputer Is Software Identical with Commercial Version

The full-scale, 16-bit LSI-11M microcomputer is the second member of



a minicomputer family that the Norden div of United Technologies, Norwalk, CT 06856 is militarizing under license from Digital Equipment Corp. Built and packaged to withstand the rigors of airborne, shipboard, ground-based, mobile, and space usages, the militarized computer, based on the LSI-11 architecture, is software identical to its commercial counterpart and four times faster.

Designed to withstand environmental extremes, the computer is manufactured under MIL-9858A control and meets key military specs. Extensive testing helps assure full compliance with military requirements.

The bus is a high speed bidirectional interface that connects CPU, memory, and I/O. Devices connected to the bus communicate directly with each other at their own rate without CPU intervention. I/O transfer rates range up to 833k words/s.

Deliveries are scheduled to begin in December. Quantity prices start at less than \$2000. Various options are also available.

Circle 184 on Inquiry Card

uProcessor System Offers Development Ease In Industrial Environments

Based on a 16-slot mainframe and Motorola chip, the 6015 processor drawer has been announced by Digimetric Co, Div of Sybron Corp, 730 Kalamath St, Denver, CO 80204 as part of the series 6000 oem microcomputer system, which enables cost-effective and rapid design and production. The device has power/fail auto restart, real-time clock and hardware priority interrupt, a loader and DEMON monitor in ROM, and 32k of static RAM. Memory is available in 2k or 8k static RAM and 4k p/ROM. Circle 185 on Inquiry Card

8k Static RAM Is Added to Family of M6800 Support Modules

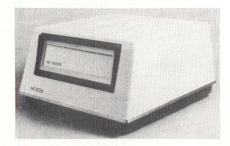
Compatible with the M6800 microprocessor bus, the 9626 fully static RAM module has been added by Creative Micro Systems, 6773 Westminster Ave, Westminster, CA 92683. Pin- and outline-compatible with Motorola EXORciser and Micromodules as well as other industry stan-

dard cards, the module provides 8192 bytes of storage and has 16-bit address decoding with fully buffered data, address, and control lines. Features include a 530-ns max access time, 8.5 W max of power, data hold time of 10 ns max, input logic current of 0.36 mA max, and single 5-V power.

Circle 186 on Inquiry Card

µComputer Aid Station Allows Simultaneous System Developments

To provide a "base" environment for one or more microcomputer systems under development, the Aid Station (XAID-100) accepts up to 13 12 x



8.5" (30.48 x 21.59-cm) cards in two groups of six and seven. Wirewrap pins on the motherboard allow for busing between the two. Included is a single 115-Vac power supply capable of supporting at least two complete systems simultaneously. Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 also offers an optional wirewrap board or an extender card for troubleshooting individual boards. Circle 187 on Inquiry Card

LSI-11 Microcomputers Obtain Fast Char Display With RAM Video Interface

The VIURAM alphanumeric video interface unit RAM for the DEC LSI-11 and PDP-11/03 is a single, dual-width board which connects the microcomputer directly to a standard video monitor. Containing a 1k x 8 static Mos RAM and positive or reverse video display format of 16 lines of 64 char/line, the interface from Computer Technology, 6043 Lawton Ave, Oakland, CA 94168 generates a standard composite video signal for visual display of characters whose ASCII codes are stored in memory.

Circle 188 on Inquiry Card

The complete \$795 graphics plotter.

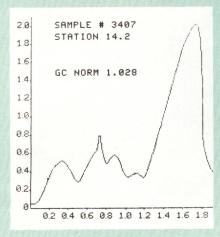
It's self contained, plots 8,192 dots per second, and is priced thousands of dollars less than others.



They said it couldn't be done!

Recently, we introduced the EX-800, a complete 80 character line printer for just \$655. Now meet the Axiom EX-810 graphics plotter, our printer's younger and smarter brother, incredibly priced at \$795!

"You can't build a plotter for \$795," we were told. But we have. Using the same simple, reliable marriage of mechanics and electronics that made our printer an instant success.



Plots fast — and prints, too

The EX-810 is a compact, selfcontained unit, designed to work with microcomputer systems. It can print 8,192 dots per second with up to 512 dots per row. Under software control, the EX-810 can also function as an 80 column alphanumeric line printer with speeds up to 160 cps.

The plotter has been designed to be driven by an 8-bit microprocessor with a minimum of software overhead. The built-in TTL compatible controller takes care of all of the timing functions required to drive the printhead and advance the printer.

The advantage of electrosensitive plotting

Electrosensitive plotting is the key to the high performance and low cost of the EX-810, because this technique is the simplest possible way to place a visible mark on paper.

The advantages are many. The permanence of the hardcopy, unaffected by sunlight, moisture, heat or age. The shelf-life is indefinite, and the high contrast makes excellent photocopies. Also,

the paper is inexpensive, and readily available, costing less than $1\ensuremath{\note}$ per plot.

Lightweight and rugged

Designed for the OEM, the EX-810, which can print forms, tickets, maps, pictures, charts, logos or anything you want, is completely self-contained including case, power supply, and paper roll holder. Weighing in at 12 lbs., the plotter is only 95%" wide, 37%" high and 107%" deep.

The EX-810 is virtually maintenance free, too. The simple, non-impact print mechanism has an amazing MTBF of 11.6 million lines, and the print-head is self-adjusting. Also, there are no inky ribbons to change.

The EX-810 graphics plotter ushers in a new era. Phone or write for OEM prices today.

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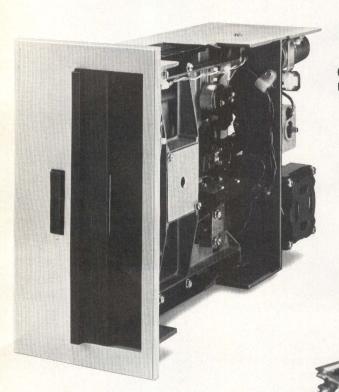
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Capacity

The SA 850/851 gives you twice as much storage capacity as a single-sided, double density drive. Yet it requires no more cabinet space. One drive packs up to 1600 kbytes unformatted, or 1200 kbytes formatted.

Double density gives you 1600 kbytes—compatible and equivalent to the newly announced IBM S/34 two-sided drive. The Shugart SA 850/851 is available now and this drive accepts FM and double density MFM or M²FM encoding.

floppy from number 1

Speed

Data access is faster, too. Just 3 ms track-to-track. Average seek time, including settling, is 91 ms. That's 71 ms faster than IBM's two-sided floppy.

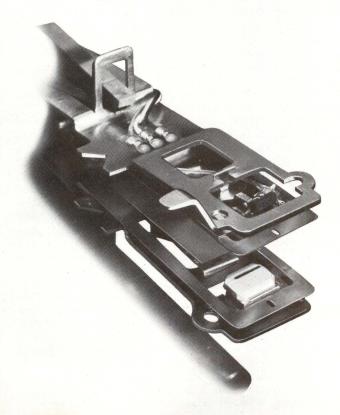
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AROUND THE IC LOOP

Semicustom Integrated Circuits-The Do-It-Yourself LSI Chips

Eric R. Garen

Integrated Computer Systems, Incorporated Culver City, California

Editor's Note: The concept behind this editorial section, inaugurated in September 1976, is to offer our readers current, valuable information through the use of a format that remains flexible at all times. To continue this policy, we are initiating with this issue a series of bylined columns that present in-depth studies of integrated circuit technology. Specific emphasis of the column will vary from month to month in order to accommodate the wide range of possible subjects. Comments and suggestions from readers will be considered for future columns.

When designing small digital systems, an often overlooked design alternative is the semicustom integrated circuit. It can fill a need in 1000 to 100,000 quantity applications for which a microprocessor design is a costly overkill and for which the development of custom large-scale integration is far too expensive. In this situation, most designs utilize discrete parts, but the semicustom large-scale integration chip may offer a more effective solution.

A semicustom large-scale integration (LSI) circuit is a standard array of cells typically comprised of transistors, gates, or functional modules such as flipflops. Additional buffer circuits for interfacing to a variety of external electrical requirements and input/output (I/O) bonding pads complete the chip. To implement a circuit, these cells are "wired" together by



Eric R. Garen is a vice president of Integrated Computer Systems, Inc (ICS) with responsibility for North American operations and for all ICS technical activities worldwide. He is a graduate of the California Institute of Technology and has both technical and managerial experience with digital systems, minicomputers, and microcomputers. During the last four years; he has conducted microcomputer courses for all levels of engineering and management.

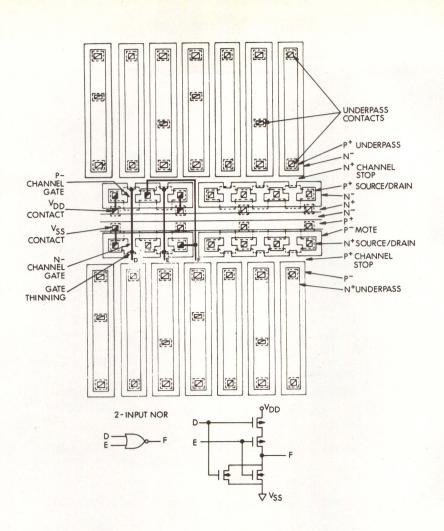
etching the final metallization layer to interconnect the cells according to the particular circuit design. One or at most two custom masks are required. Thus, implementing semicustom LSI is far quicker and less expensive than true custom LSI, because all but the final fabrication steps are identical for all parts.

Typical costs, working from a schematic to develop prototype parts, range from \$3000 to \$10,000, a far cry from the \$30,000 to \$200,000 required for the truly custom integrated circuits (ICS). Furthermore, the turnaround is four to ten weeks for semicustom chips versus the 4- to 12-month development cycle for a custom IC.

This cost advantage for semicustom chips is especially true at the lower quantities but diminishes as the total number of chips per year rises. As shown in Table 1, semicustom offers a cost advantage of approximately \$35,000 at 10,000 units; however, with 100,000 the two are almost equal. Prices listed are only a rough estimate of actual costs. The crossover point between custom and semicustom will vary from as low as 50,000 units to nearly 250,000 units per year depending on application and manufacturer, and other such variables.

Of course, most designers who have used semicustom chips would never have considered custom LSI in the first place. They used semicustom chips to replace discrete logic. In many applications the most important advantage has been space reduction. The most often used semicustom chips typically replace between 10 and 50 small-scale/medium-scale integration (ssI/MSI) packages. Second most often cited advantage of semicustom chips is low power consumption (current requirements vary from 1 to 30 $_{\mu}\mathrm{A/gate}$). Improved reliability is also of prime importance, especially for field portable applications.

Of course semicustom chips would not be attractive if their costs were not equivalent to or less than those of discrete parts. Based on chip costs alone, semicustom parts which cost \$2.50 to \$10 each have difficulty when compared to a mix of \$0.15 gates and \$0.30 msi. However, cost improvement is typically obtained by reduction of overall manufacturing costs. Incoming inspection is reduced to a single chip. Testing and rework costs are obviously far less and warranty costs are similarly reduced. An important but intangible benefit to most manufacturers is the ability to keep their circuits proprietary, a major advantage over discrete logic.



Basic cell of an International Microcircuits MasterMOS chip. An entire "medium" size chip of this type contains 254 p- and 254 n-channel MOS transistors together with interconnection underpasses and buffers to external circuits. Each cell is built around power buses for $V_{\rm DD}$ and $V_{\rm SS}$. Just above and below these buses are seven p- and n-channel field effect transistors (FETs) arranged in groups of three and four. Above and below these are rows of underpass interconnections that allow 2-dimensional interconnection between transistor circuits. Interconnections between elements are made through contact openings represented by small squares containing diagonals. A simple 2-input NOR gate is shown constructed by connecting two n-channel FETs in parallel and two p-channel FETs in series. Note that $V_{\rm SS}$ connects to source of n-channel FETs and $V_{\rm DD}$ connects similarly to p-channel FETs. Input lines D and E interconnect the gates of their two complimentary FETs while F output line connects drains

The possible problems in using semicustom circuits are commercial in nature. First, the user must be willing to commit his design to volume purchase. To correct a mistake, the price is high—not unlike the dilemma of designing with masked read-only memories (Roms) vs programmable Roms (p/Roms). The second problem is the lack of second source parts. With the exception of the Interdesign linear chip, which is second sourced by Exar Integrated Systems, the chips are single source. Keep in mind, however, that the companies applying semicustom parts are actually made up of

TABLE 1 Comparison of Development Costs For Custom and Semicustom Chips

	Full Custom Cost 10k 100k		Semicustom Cost 10k 100k	
Type of Cost	Chips/Yr	Chips/Yr	Chips/Yr	Chips/Yr
Development	\$40,000	\$40,000	\$6500	\$6500
Price/part	\$9.50	\$6.50	\$9.50	\$7.00
Total	\$135,000	\$690,000	\$101,500	\$706,000

TABLE 2
Summary of Semicustom LSI Circuits

Manufacturer	Technology	Component ¹ Range	Design Cost ²	Part Cost ⁸
Exar Integrated Systems 750 Palomar Ave PO Box 6229 Sunnyvale, CA 94088 (408) 732-7970	IIL (864 gates + 88 transistors	\$7000 to 12,000	\$6 to 10
		272 gates + 20 transistors	4000 to 8000	5 to 8
	Bipolar, linear	69 to 93 transistors	2500 to 4000	3 to 4
Ferranti Electric E Bethpage Rd Plainview, NY 11803 (516) 293-8383	Bipolar, linear, and/or digital	225 gates	10,000 typ	10 typ
Interdesign 1255 Reamwood Ave Sunnyvale, CA 94086 (408) 734-8666	Bipolar, linear	30 to 93 transistors	4800	0.95 to 8
	Silicon gate n-MOS	262 gates	4800	5 to 8
International Microcircuits	CMOS	50 to 200 gates	2650 to 4150	2.50 to 10.05
3004 Lawrence Expwy Santa Clara, CA 95051 (408) 735-9370		400 to 800 gates	9600 to 19,000	27.80 to 64.50
Master Logic 761 E Evelyn Ave Sunnyvale, CA 94086 (408) 732-7777	CMOS	50 to 200 gates	4200 to 8600	3.50 to 13.50
Microcircuits Technology 975 Comstock St Santa Clara, CA 95050 (408) 248-1101	Silicon gate n-MOS	220 to 1150 gates	5000 to 14,000	5.60 to 18.50
	CMOS	80 to 480 gates	2900 to 12,500	3.70 to 17.40
Stewart Warner 730 E Evelyn Ave Sunnyvale, CA 94086 (408) 245-9200	IIL	208 to 408 gates	3800-4350 (customer does layout)	1.42 to 3.97

¹The term gate is defined as a NOR or NAND logic element. One manufacturer's chip contained wired flip-flops. These were counted as five basic gates

These figures represent a range of possible costs for the various size devices offered. They assume that the customer supplies the manufacturer a breadboard-tested schematic or logic diagram and that the manufacturer supplies the customer a specified quantity of tested prototype chips. Some manufacturers permit the customer to do layout, whereas others perform layout as part of the development. One manufacturer noted in the table requires that the customer do the layout The figures quoted are for 10,000 pieces mounted in plastic DIPs

engineers and contractors who design and then subcontract the actual fabrication of the parts to many different semiconductor manufacturers. Thus, multiple production facilities do exist for each part.

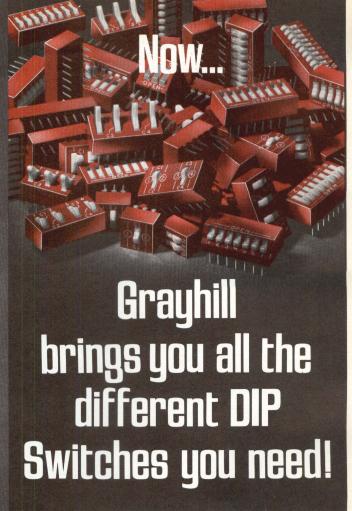
To use a semicustom ic the designer has two alternatives. First, he can simply mail his schematic to the semiconductor manufacturer who will do the layout. Typical costs for this service are \$600 to \$2000 and require two to five weeks, depending on the complexity. Because of the relatively low cost, most users (about eight of ten) take this approach. The second alternative is a "do-it-yourself layout." Designers are provided

with kits and manuals which describe standard functional elements including functional equivalents of most ssi and MSI parts. For the analog designer, amplifiers, oscillators, and other circuits form the basic building blocks. Thus, layout is typically a matter of organizing the module arrangement for easy internal interconnection (not unlike laying out a standard printed circuit (PC) board).

An example of a section of a semicustom chip is shown in the Figure. The designer transfers his logic diagram onto the semicustom chip by constructing the various logic elements of his logic diagram on the chip First...



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Toggle DIP[®] available with SPDT circuitry, 2, 3 or 4 stations; DPDT with 1 or 2 stations.

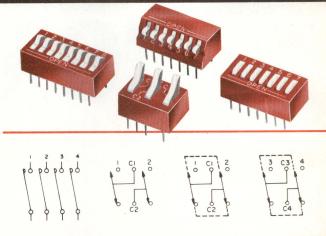
Piano DIP[®] (side actuated) from 4 to 10 stations, SPST circuitry under each rocker.

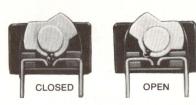
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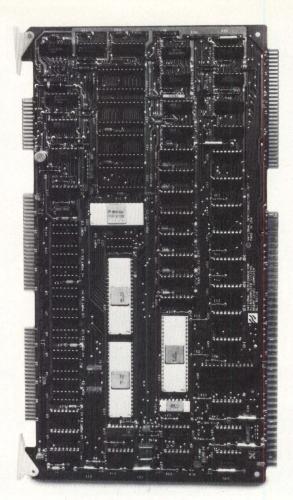
Different delivery standards, too

Most Grayhill DIP Switches are available off the shelf in production quantities from Grayhill or its nationwide distributor network.



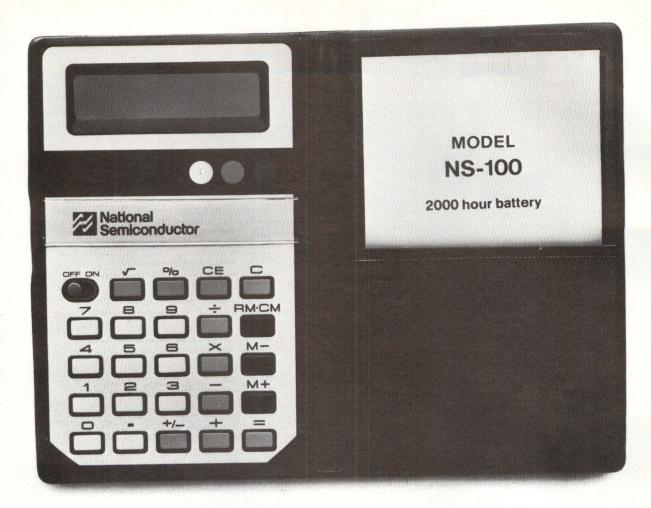


For detailed information on Grayhill DIP Switches, consult *EEM* or write for Bulletin#276 to Grayhill, Inc., 561 Hillgrove Ave., La Grange, Illinois 60525, phone: (312) 354-1040.



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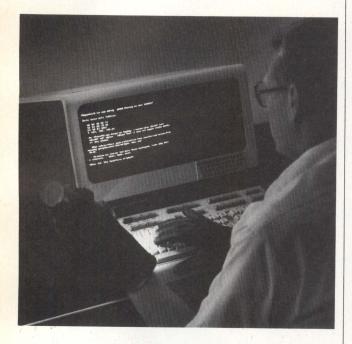


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drawing, as illustrated. When all elements of the logic diagram have been created on the drawing, the elements are interconnected in much the same manner as PC board interconnection lines are run.

Most semicustom houses will check the layout by hand; some use computer simulation to find less obvious design flaws. Note that an error means a second mask which is typically charged (about \$500) to the person doing the layout. Thus, if the semiconductor company made the error, that company corrects it at no charge.

Semicustom chips are available in several technologies (Table 2), each requiring a specific fabrication technique and also differing in physical appearance. Complementary metal-oxide semiconductor (cmos) and n-channel mos (n-mos) devices are voltage driven while integrated injection logic (IIL) and bipolar transistor-transistor logic (TTL) are current driven. Generally, bipolar and IIL devices are faster than the two mos devices, but both bipolar and IIL devices require higher power to achieve the higher speed. Similarly, speed of the cmos type devices can be increased by increasing voltage, likewise resulting in higher power requirements.

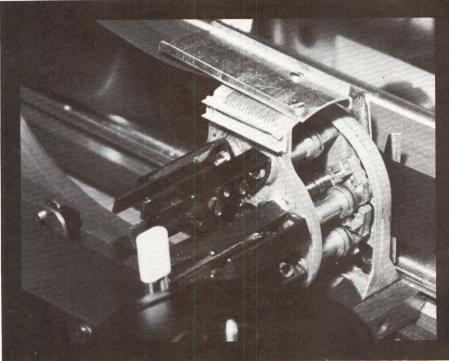
As a comparison to demonstrate the differences in speed, consider a gate on each chip type that fans out to four gates. Typical propagation delays through the gate for each of the four technologies as applied to existing semiconductor chips are bipolar TTL, 10 ns; IIL, 50 ns; CMOS, 70 ns; and n-MOS, 100 ns. What is important is the comparative differences in speed rather than the actual speed difference. As a point of caution, however, these numbers must be regarded as generalities rather than absolutes, because there are ways in which the differences in speed can be minimized by the various technologies. For instance, n-MOS can be made to operate at speeds comparable with CMOS and IIL.

Two other variables that distinguish the various technologies are packing density and power consumption. The density advantage goes to IIL and n-Mos, which have similar packing densities, followed by bipolar TTL, which is followed by CMOS. CMOS has the lowest density because it requires more transistors to create a logic function than any of the other technologies. For applications requiring battery-powered operation, of course, a CMOS type semicustom chip is almost always chosen because of its low power requirements as well as the noise immunity characteristics.

Manufacturers of both digital and linear oriented chips have seen more use of the linear circuits principally because of the availability of alternative LSI solutions to digital problems. Most applications have been in the 5000 to 50,000 quantity range although many applications require only 1000 devices. Communications applications lead the field with literally dozens of different circuits being supplied for modems and for handheld and mobile radio equipment, which uses chips for encoders, decoders, auto identification systems, and channel scanners. Amateur radio equipment utilizes semicustom chips for automatic Morse code generation. Portable instrumentation uses have also been numerous. They take advantage of the small space, light weight, and low power of these chips. A typical example is an "on-board" continuous pulse rate monitor for cardiac rehabilitation patients.

Will a semicustom chip work for a particular design? It should definitely be considered if the volume is in excess of 1000 parts; if space, power and reliability are of primary importance; and if reduced electronics manufacturing cost will have an important impact on the cost of the final product.

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LSI Interface Chip Assumes Main Processor ALU Responsibilities

Memory interface function MS10803 is a 4-bit wide MECL LSI chip which generates memory addresses, provides for transfer of data to and from a main processor, and permits arithmetic, logic, and shift operations to be performed on any data or address moving through the function. Containing its own arithmetic and logic unit (ALU), the device performs a total of 13 basic ALU functions on seven possible operands and carries out 17 data transfer operations.

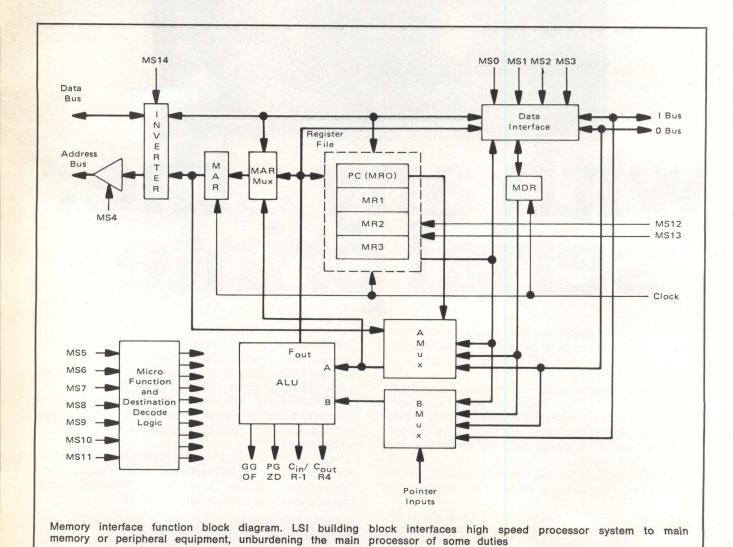
This computational capability allows several modes of memory addressing (eg, relative, indexed, extended, indirect) to be performed. Moreover, it is also possible to con-

trol the program counter or to do stack push/pop operations on the chip, thereby potentially unburdening a main processor.

In a typical application, the function interfaces a high speed processor subsystem, such as the MC10800 4-bit ALU slice, to system main memory or peripheral equipment. Connected in parallel with a processor, it permits double-precision arithmetic and, in larger systems, a number of the functions can be connected in parallel to drive multiple 1/0 ports. In peripheral controller systems that perform high speed data transfer operations but do not need the computational power of a complete bit slice ALU, the function can be used as an ALU and as interface logic to reduce the controller part count. In still other applications, the device

can be used as a microprogram controller with internal ALU used for relative addressing; here it generates addresses for control memory rather than main memory and uses its internal registers for storing subroutines.

The memory interface function contains six 4-bit registers, an ALU with microfunction and destination decode logic, and data interface logic. These perform the three major tasks of the device: generate memory addresses, route incoming and outgoing data through the function, and perform arithmetic, logic, and shift operations on data moving through the device. Data move into and out of the function via five separate 4-bit ports. Both data transfer and computation within the device occur in response to commands applied to 15 select



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lines on the chip labeled MS0 through MS14 (see diagram). In addition, ALU conditions (such as group select, group propagate, and zero detect) are flagged at two input pins while carry-in, carry-out, sign-bit, shift-in, and shift-out signals are transferred via two other pins.

Three of six memory interface function registers are given functional designations: memory address register (MAR), memory data register (MDR), and program counter (PC). The remaining three, along with the program counter, are referred to as the register file and can be used as stack pointer, index register, or other memory related functions; no fixed register assignments exist in the register file. Five 4-bit ports bringing data onto or moving data out of the function are input bus (I bus), output bus (O bus), data bus, address bus, and pointer inputs.

Fifteen pins accept command input to the memory interface function. Of these, four (MS0-MS3) tie to the data interface. Levels on these lines in conjunction with levels applied to two other inputs (MS5 and MS14) route data throughout the chip. A total of 16 different transfers can be produced by combinations of levels on these inputs: transfers between the ALU and the input bus and memory data register; transfers between the input bus and memory data register; transfers between the output bus and memory data register and register file registers; and transfers between the data bus and each of several registers and buses (register file registers, memory address register, memory data register, input bus, and output bus). Some transfers call for inversion of data being transferred. This is accomplished by applying a logic 1 (non-inversion) or 0 (inversion) to the input labeled MS14.

Of the remaining eight pins accepting command input to the chip, MS6 through MS11 control ALU operand and function selection. MS6, MS7, MS8, and MS9 specify one of 13 arithmetic, logic, or shift operations: add, subtract, arithmetic and logical left shift, arithmetic and logical right shift, and, or, two types of exclusive-or, modify (modify address register contents), pointer (modify contents of register file register, memory data register, output bus, or program counter), and relative (modify program counter contents). Mod-

ify, pointer, and relative commands provide addressing capability to the device.

MS9 also controls the ALU status outputs while MS10 and MS11 specify which operands are to be used for a given operation. For example, with the arithmetic left shift, the two inputs can specify that the shift occur on data from the output bus or data in the memory address register, memory data register, or register file register. Of the last three pins accepting command input, MS12 and MS13 specify which register file register to access for a given operation (MR0-MR3), while MS4 enables or disables the address bus.

In addition to the 15 pins bringing command input into the memory interface function, four other pins carry status and data bits in and out of the device during command execution: carry in/right shift LSB ($C_{\rm in}/R1$), carry out/right shift MSB ($C_{\rm out}/R4$), group propagate/zero detect (PG/ZD), and group generate/overflow (GG/OF). Which of two conditions possible on a given pin is present at a point in time depends on the command being executed.

The MC10803, manufactured by Motorola Semiconductors, PO Box 20912, Phoenix, AZ 85036, is directly compatible with all devices in the MECL 10,000 series. Housed in a 48-pin quad-in-line package, the device is available from factory stock at a price of \$40 in 100-unit quantity. Circle 350 on Inquiry Card

Companding DAC Conforms To European PCM Law Characteristic

Claimed to be the first monolithic companding D-A converter to conform with the CCITT exponential "A" law characteristic used for European pulse code modulation (PCM) systems, the DAC-87 functions as an expanding D-A converter (decoder), can be configured in a compressing A-D converter (encoder), or may be timeshared between encoding and decoding functions. To implement the "A" law characteristic, the device affords a sign plus 7-bit word, which, excluding sign, contains three bits that specify one of eight binary-related chords and four bits that specify one of 16 linearly-related steps. Chords and steps specify a point on the "A" law exponential curve.

In the "A" law, steps in the first two chords are the same size, while steps in the remaining chords are a binary progression of the first chord's step size; third chord's steps are twice the first's, the fourth's four times the first's, etc. In addition, the law requires the decoder output to be a a half-step higher than the encoder's for any given code.

Manufactured by Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050, the device is a multiplying D-A converter in which the output current is the product of the normalized digital input and the input reference current, thus ensuring true current source outputs with —5- to 18-V compliance. In most applications, the relationship between input reference current and the full scale output current eliminates the need for reference current trimming.

Primary application is in PCM carrier systems, digital PBX and key systems, electronic central offices, and satellites. Because of its 8-bit word size, which permits a 66-dB dynamic range plus sign, the device serves well in microprocessor-driven applications that conform to the "A" law characteristic.

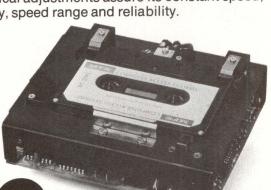
For the E (and C) versions, resolution is ±128 steps, maximum nonlinearity is ± 0.5 (± 1) step, max full scale drift is ± 0.25 (± 0.5) step, and max chord endpoint accuracy is ± 0.5 (± 1) step. Full scale current deviation from ideal using a 10.000-V reference input with appropriate input resistance measured at 25°C is ± 0.5 (± 1) step. Settling time to within ±0.5 step is 500 ns typ, full scale drift over the full 0 to 70°C operating temperature range is ±0.05 (± 0.1) step, and max output voltage compliance for a full scale current change of ≤0.5 step is 18 V. Typical power dissipation is 167 mW.

D-A conversion (see decode connection diagram) may be illustrated using an operational amplifier connected to the decode outputs as a balanced load. The decode mode of operation is selected by applying a logic 0 to the encode/decode pin of the device. This enables the decode pair output, disables the encode pair output, and allows direction of output current flow to be determined by the sign bit input.

When the sign bit input is high, a positive voltage is produced at the operational amplifier's output. A low on the sign bit input forces a negative amplifier output. Each 8-bit digital input including sign specifies chord and step of a digitized point on an analog signal. Thus with each input, the DAC produces a corresponding section of an analog signal at the operational amplifier output

Have it your way!

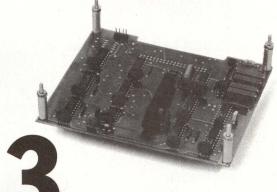
Start with our 250B cassette tape transport for \$525.*
More than 28,000 are at work almost everywhere. These are 1/3 the size of a minifloppy, have a 1/108 error rate, 366 kilobyte storage, and a 32 kilobit transfer rate. Just 2 moving parts and no mechanical adjustments assure its constant speed, accuracy, speed range and reliability.



Add a serial interface board for \$150.* Board #1 has Bi Ø level (The ANSI/ECMA std), write oscillator, 4 programmable speeds and gap detector electronics, plus BOT/EOT optical latch.

Or go all the way up to our Model 500 Intelligent Data Buffer for \$1995.* We packaged the 250B with a powerful microprocessor, operator/ remote controls, and EIA-RS232C or TTY interfaces for unmatched terminal enhancement! The 5000 provides data string search, 13 selectable control codes, extensive validity checking (RAW, CRC and Parity), automatic diagnostics, auto answer, 202 modem control and 86/138 character block select as standard features.





Or add an 8 Bit parallel board for \$325.* Board #2 includes all the Board #1 goodies plus an LSI USRT and other IC's for parallel/serial/parallel data I/O.



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*Prices substantially lower for quantity purchasers.

Is your computer smart enough



One DC-300A cartridge equals almost 16 feet of cards

Or hundreds of feet of paper tape.

And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

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It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3M DC-300A data cartridge.

With cartridges, you can store all of your

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need for cards or paper tape. Your filing system is simplified and overhead is

greatly reduced.

Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need Cards must be read one at a time. never touch the media. It's well

A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

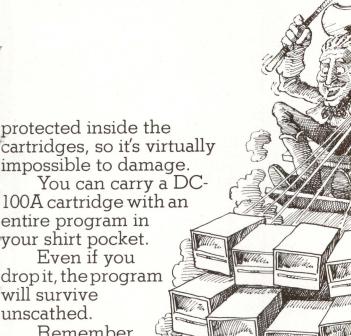
And, if you'd take the time to ask it, your a computer would probably tell you so. It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



to choose our cartridge drive?



One formatter can control eight drives at once.

cartridges, so it's virtually impossible to damage. 100A cartridge with an

entire program in your shirt pocket.

drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards.

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

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Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our

unique DCD-1. It offers many of the features of our bigger systems, vet it will fit inside a five-inch cube.

The cartridge alone measures just 2.4 x $3.2 \times .5$ inches.

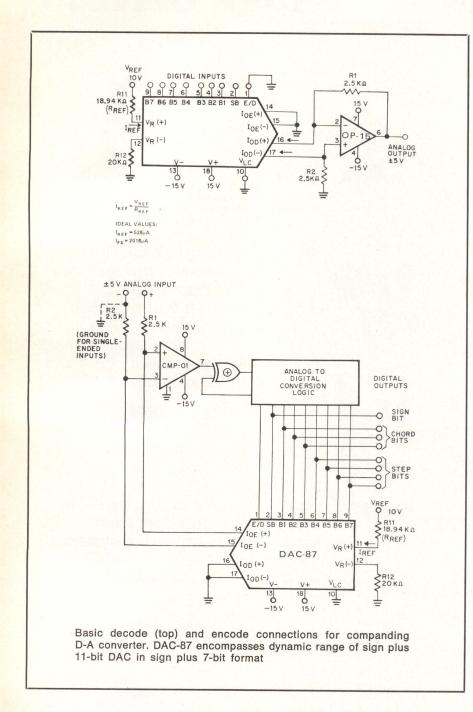
See for yourself.

Send us the coupon. There's much more we can tell you about our drive systems.

Study the information carefully. If your computer isn't smart enough to choose our drive systems,

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which accurately represents the polarity and magnitude of the original signal.

Compressing A-D conversion (encode diagram) requires a comparator tied across the DAC encode pins which are connected, in turn, with a sample-and-hold amplifier. The comparator connects to an exclusive-or that supplies input to and receives input from a successive approximation register. The register is tied to the eight output pins of the DAC. This junction also affords parallel output

from the entire encoder function. A serial output from the encoder is supplied from the register.

An encoding sequence begins with the sign bit comparison and decision of the analog input from the sample-and-hold amplifier. During this time, the comparator is only a polarity detector. The encode/decode (E/D) input is held at a logic 0. Therefore, no current flows in either encode input. Once the input polarity is determined, the E/D input is changed to a 1, thus allowing current

to flow into the encode input selected by the sign bit.

For the positive portion of an analog signal, current flows into the DAC's positive encode input pin through a resistor at the comparator input. The resulting voltage drop across the resistor is compared to the analog signal and the comparator output is entered in the successive approximation register during seven successive comparisons. For the negative portion of an analog input, current flows into the DAC negative encode input pin through another resistor at the comparator input which develops a negative voltage that is compared with the analog input. Again, the comparator output is entered in the successive approximation register during seven comparisons. The result of the successive comparisons for a given analog input from the sample-and-hold amplifier is a digital value detailing polarity and magnitude of the incoming analog signal.

The DAC-87 is available in an 18-pin hermetic DIP and interfaces with DTL, TTL, MECL, or CMOS logic inputs. DAC-87EX sells for \$9.90 and DAC-87CX for \$9, both in quantities of 100

Circle 351 on Inquiry Card

12-Bit Accumulating Multiplier Both Adds and Subtracts

Multiplication of two 12-bit operands to produce a 27-bit product in 175 ns is now possible with the TDC-1003J bipolar multiplier. Moreover, the multiplier can sum successive products from an accumulated total. One other function the multiplier chip performs is a true rounding of the lower 11 bits of a product into the product's upper 16 bits.

Because of its speed, and summation and subtraction capability, which allow it to easily carry out multiplication of complex numbers, the multiplier is well-suited for digital filter applications, particularly fast Fourier transform filters and recursive and nonrecursive filter elements. Faster than equivalent MSI multipliers, the device also serves high speed signal processing applications in such areas as telecommunications.

Two operands enter the multiplier via the X and Y registers and are multiplied when an input to the multiplier chip labeled Start Acc (diagram) is presented with a logic high level. The two operands are multiplied in the chip's asynchronous

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

Like plotting capability ... at no extra cost.

It would seem enough to find a 132 column, 300 lpm printer with print quality others can't match, with an elegantly simple mechanism that assures a greater MTBF, and a modular design that dramatically cuts MTTR. The Printronix 300 offers all of these advantages.

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Because of its unique mechanism, it can put a single dot anywhere on paper. It forms characters a dot row at a time when printing. In the plot mode, it can form any pattern a dot at a time upon command. Drawings. Graphs. Bar codes. Large character labels. You name it and you can do it on a Printronix 300.

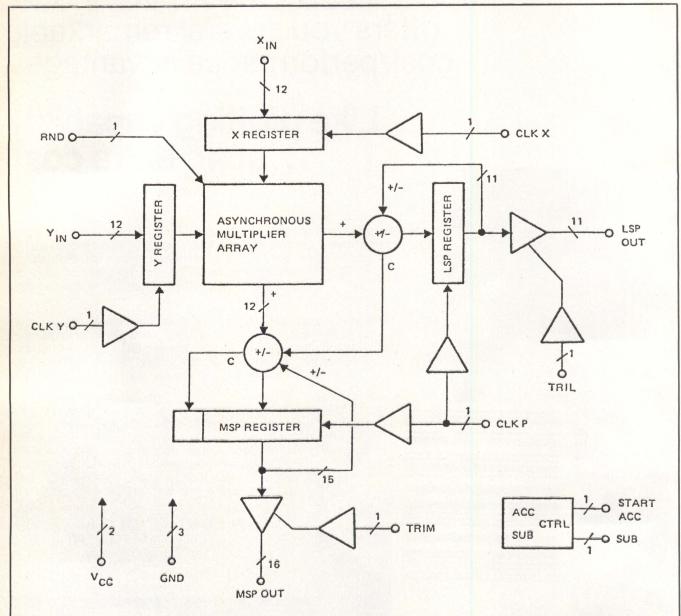
It's a handy capability to have around, and it comes to you with our compliments . . . at no extra charge . . . along with the other remarkable advantages that make the Printronix 300 your best buy. Send for our brochure. You'll discover why the Printronix 300 prints better, will last longer, and require far less maintenance. That's why it's been sold with a one-year warranty from the beginning.

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Logical block diagram for TRW 12-bit multiplier. Multifunction arithmetic unit performs 12 x 12 multiplication with 27-bit accumulation capacity

multiplier array and the resulting 27-bit product is moved into the multiplier's LSP (low order bits) and MSP (high order bits) registers.

Loading two more operands in the X and Y registers and applying a low level to the Start Acc input produces a product from the multiplier array which is summed to the present contents of the MSP and LSP registers. Loading two more operands in the X and Y registers and applying a low level to the Start Acc input while placing a high level on the

chip input labeled Sub produces a product from the multiplier array which is subtracted from the present contents of the MSP and LSP registers. To round the LSP contents into the MSP register requires a high level on the input labeled Rnd.

The LSP and MSP registers produce an output via lines labeled LSP Out and MSP Out, respectively, when appropriate levels are applied to input lines labeled Tril and Trim. These and all other input and output lines are TTL-compatible.

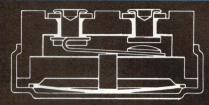
Supplied in a 64-pin DIP, the TDC-1003J, which is produced by TRW Inc, One Space Park, Redondo Beach, CA 90278, includes an integral heat sink and operates from a single 5-V supply over the 0 to 70°C temperature range. Current price for the chip in a 64-pin package is \$150 in 100 to 499 quantities and delivery is from factory stock. By the fourth quarter of 1977, a full military temperature range version will be available.

Circle 352 on Inquiry Card

Elmwood makes Sense

Why overspecify? Choose the fast-response snap-acting Elmwood thermostat model that just fits your needs. Choose the levels of tolerance and differential that are right for your product, without wasted details or dollars.

For worldwide sales many Elmwood models meet CSA and European requirements (and DIN norms), as well as U.L. Ratings are to 15 amps, for exposures -65°F to 550°F (-54°C to 288°C), and each unit is factory pre-set, tested and tamperproof. Doesn't Elmwood make Sense? Ask for prototypes.



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Precision Controls
CIRCLE 80 ON INQUIRY CARD



Schottky Cell Array **Technology Provides Custom LSI Chip**

A monolithic IC containing a custom interconnected array of up to eight cells, each the equivalent of a standard 54LS MSI or SSI low power Schottky device, SCAT (Schottky cell array technology) provides an alternative to custom LSI. Like custom LSI, it affords reduced mounting requirements, increased reliability by reducing part count, and a proprietary part-but at typically one-fourth the cost and development time of custom LSI. Moreover, the design iterations typical of custom LSI are minimized with this chip since all cells have been previously characterized, thus leaving only the custom interconnection to be proven.

Creating the custom chip begins with the designer supplying the manufacturer, Hughes Aircraft Co, Microelectronics Products Div, 500 Superior Ave, Newport Beach, CA 92663, with a breadboard prototype of the design to be implemented. This breadboard is constructed with standard 54LS Schottky devices for which equivalent cells exist; the designer can choose from a wide range of MSI/SSI gates, counters, flipflops, arithmetic elements, and shift registers contained in the manufacturer's cell library.

Once the prototype is supplied, equivalent cells needed to implement the design are arranged in an optimum configuration within a 2 x 2,

2 x 3, or 2 x 4 cell array. Then, using two layers of thin film metallization, the various elements of each cell, gate, flip-flop, and counter are interconnected in a manner similar to routing on a 2-layer PC board. To facilitate interconnection, a cell has one to four rows of evenly spaced 1/o pads with more complex cells having two additional layers of aluminum metallization to interconnect the 1/0 pads of the basic cells.

Since all cells are fully characterized and the layout details of each are stored as a set of standard 10X reticle photoplates for mask generation, development is limited to designing the interconnection layers and fabricating the various masks. A computer graphics system digitizes the interconnection data for generation of the 10X reticle masks. Once development is completed, prototype chips are produced, tested, and sent to the customer for evaluation. Following evaluation, a production run of the part occurs.

The basic cell measures 80 x 137 mils, small enough for a maximum of eight to be arranged on a 326x 280-mil chip. Plans are presently being made to reduce cell and chip size by approximately one-half, with the amount of logic on each cell remaining the same. The chip comes in a variety of packages: leadless, DIL, and flatpack styles, with each containing up to 64 pins.

Development costs for a chip and a quantity of prototype chips is in the neighborhood of \$12,000. Production runs of 10,000 chips produce a cost of roughly \$30/chip for ceramic parts with plastic parts available at lower cost.

Circle 353 on Inquiry Card

Dual 4-Input Gate Provides 550-ps Switching Speed

Fully ECL III- and ECL 10k-compatible, the SP16F60 dual 4-input or/nor ic has a typical 550-ps switching speed. Because of its low input loading factor, 1, and high output loading factor, 70, the device provides high fan-in and fan-out. On input, 50-kΩ input pulldown resistors allow the gate to be used with openended inputs; while on output, it can drive a $50-\Omega$ line.

Operating with an 8-V positive difference between Vcc and VEE, the IC contains two diodes which provide temperature compensation to ensure that the threshold of the device is always in the center of the transition region over the full -30 to 85°C temperature range. During operation, power dissipation is typically 120 mW in a no-load condition.

The gate, offered by Plessey Semiconductors, 641 Kaiser Ave, Irvine, CA 92714, serves the high switching speed requirements of such applications as data communications, instrumentation, and PCM transmission systems. It is available in a ceramic DIP at a 100-up price of \$12 with delivery off-the-shelf.

Circle 354 on Inquiry Card

50-MHz PLL Enables TTL Input and Output

Operating with a single 5-V supply and capable of directly interfacing digital logic, the NE564 phase locked loop (PLL) can be used to synchronize



disc and tape drive mechanisms and phase locking system clocks so that one serves as back up for a second. For pulse code modulation telemetry receivers and repeater systems, the PLL facilitates bit synchronization.

In typical analog applications, its 50-mHz operating frequency permits the PLL to function very well in high speed modems, FSK transmitters and receivers, frequency multipliers, and signal generators. A more specific application finds the PLL serving as a noise filter for regenerating weak signals buried in noise.

The ability to serve this wide range of applications is due to components of the PLL hardware which comprises a voltage controlled oscillator (vco), limiter and phase comparator, and post detection processor containing a dc retriever and Schmitt trigger. Emitter coupled transistors form the vco to afford high frequency operation, while a variable free

running vco frequency is obtained by allowing an external capacitor to determine the frequency. In addition, frequency drift in the oscillator is minimized by a temperature compensating circuit.

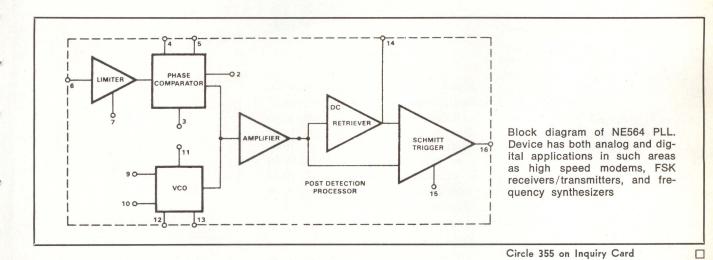
Like the vco, the limiter and phase comparator contain distinctive components. Schottky clamped vertical pnps in the limiter enable TTL-compatible input. Besides this, the limiter, in conjunction with a double balanced modulator in the phase comparator itself, accepts an external current input that can vary loop gain. For FSK signaling, the phase comparator accepts a reference voltage representing the average value of the incoming FSK signal from the post detection amplifier. This prevents any drift in the vco frequency from producing errors in the PLL's digital output.

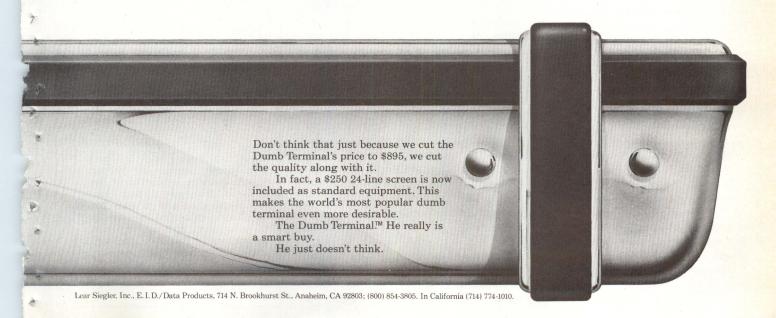
Uniqueness is also present in the dc retriever and Schmitt trigger in

the post detection processor. The de retriever demodulates FSK signals and serves as a filter for linear FM demodulation, while output signal jitter is eliminated by the Schmitt trigger's adjustable hysteresis.

With a free running vco frequency of 5 MHz, the PLL has a lock range of 40% typical, a frequency drift of 400 ppm/°C, and a typical 3%/V frequency change due to a 4.5- to 5.5-V supply voltage change. Moreover, the output voltage linearity of the PLL is 3% with signal-to-noise ratio of 40 dB and AM rejection of 35 dB. Capable of a maximum power dissipation of 400 mW, the device operates off a supply voltage that can vary from 4.5 to 12 V over a temperature range of 0 to 70°C.

A product of Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the NE564 is available in a 16-lead pinout package. Price in 100-up quantities is \$4.25.





PRODUCT

Communications Processor Fulfills

A truly universal data communications processor, Datamax 6 is supplied by Telcon Industries, Inc as a turnkey unit that connects directly to a phone line. Modem, controller boards, solid-state memory, multichannel port boards, video boards, and floppy disc plug into the unit's card file which provides a mother-board bus. The user adds only the specific software program required for a particular application; identical hardware units can perform entirely different jobs, each with its

Basic control of data flow is maintained by a microprocessor (6800 or Z80, depending on user preference) as dictated by the resident software program. Control programs are stored in electrically programmable readonly memory (EPROM). Temporary storage for contents of processor registers is provided by semiconductor random-access memory (RAM) and additional storage can be supplied with an optional floppy disc.

proper, dedicated software program.

Several variations of serial and parallel data input/output (I/O) ports are provided through interface boards. Data rates are accommodated up to 9600 baud.

The system can be supplied either with full program to meet specific application requirements or users can do their own programming. Editor/assembler, utility programs, EPROM programmer, and logic analyzer are also available.

Hardware Description

Four configurations of the basic system are offered: the PRH-30, for 8.75" (22.2 cm) rackmount, containing room for 10 pc boards and a 10-A power supply, PRH-32, 5.25" (13.3 cm) rackmount, with five board spaces and a 6-A supply; PRH-34, a desktop unit, with four board spaces and 6-A supply; and DM-60, for wall mounting, with six board spaces and 3- or 6-A supply.

Motherboard bus arrangements can be split. For instance, the 10board unit can function with 10

Multiplicity of Duties Under Program Control



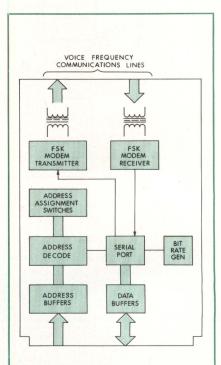
boards for one system, five each for two systems, or two each for five.

Rackmount and desktop units ordinarily include a front panel for control and I/O connections. However, this panel can be replaced by a combination floppy disc/control panel that accepts either Shugart or Wangco drives.

Microprocessor Controller

All logic and control functions are handled by a microprocessor board containing either 6800 or Z80 (8080 software-compatible) microprocessor, up to 4k x 8 of EPROM, up to 512 x 8 of RAM, and all other support devices. Parallel I/O of 16 data lines and four handshake lines are provided by a peripheral interface adapter which can be instructed by an initialization routine in the control program to configure any of the 16 lines for input or output use.

A serial data I/O port can be configured by the control program for compatibility with the majority of communications line formats. Character code sets of five up to eight bits are supported, each with selection of odd, even, or no parity. Each port can be used for asynchronous, synchronous, or isosynchronous data with clocking from an internal bit



1200/1800 modem with I/O port. This board, typical of modem boards available for Datamax 6 system, provides serial I/O port microprocessor card and a Bell 202-compatible 1200/1800-baud modem for transmitting and receiving serial asynchronous data over dedicated and dial-up telecommunications facilities

\$24.95 PROBE?

You bet! Meet CSC's Multi-family Logic Probe 2.

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Wherever you need fast, safe, accurate digital testing—you need CSC's new LP-2. It's a compact, enormously versatile circuit-powered unit that's become indispensable. As a level detector. Pulse detector. And pulse stretcher.

Easier to use. Set LP-2's switch to the proper logic family, connect two clip-leads to the circuit's supply, touch the probe to the node under test—and you get an instant picture of circuit conditions. Separate LED's indicate logic "1", logic "0", and all pulse transitions. And a 300K-plus input impedance insures minimum circuit loading.

At just \$24.95*, you don't have to think twice about owning the LP-2. Especially when you see how it simplifies testing, debugging and servicing all types of digital circuits. See your CSC dealer today. Or call 203-624-3103 (East Coast) or 415-421-8872 (West Coast) for the name of your local stocking distributor and a full-line catalog.

Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels for greater versatility. CMOS position also compatible with HTL, HiNIL and MOS logic.

PULSE LED – Indicates positive and negative pulse and level transitions. Stretches pulses as narrow as 300 nanoseconds to full 1/10 sec. (10Hz pulse rate).

HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity.

Interchangeable ground-lead connection— Provides ground-side input connection via optional cables.

Interchangeable/probe—tips—Straight tip supplied; optional alligator clip and insulated quick-connecting clip available.

Plug-in leads – 24" supplied, with alligator clips. Virtually any length leads may be connected. – –

Specifications

Input impedance better than 300Kn
Thresholds (switch selectable) DTL/TTL

logic 1 thresholds (HI-LED) logic 0 thresholds (LO-LED)

 $2.25V \pm .10V$ $0.80V \pm .05V$ HTL/CMOS 70% Vcc ± 10% 30% Vcc ± 10%

Min. detectable pulse width 300nsec.

Pulse detector (PULSE LED) 1/10-sec. pulse stretcher makes high-speed pulse train or single events (+ or - transitions) visible Input protection overload, ± 25V continuous; 117 VAC for less

than 10 sec.; reverse-polarity, 50V

Power requirements 5-15 volts Vcc; 30mA max.

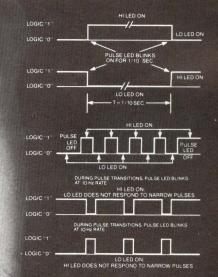
Operating temperature 0-50°C

Physical size (I x w x d)

5.8 x 1.0 x 0.7" (147 x 25.4 x 17.8mm)

Weight 3oz. (.085Kg)

Power leads detachable 24" (610 mm) with color-coded insulated clips; others available



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CIRCLE 82 ON INQUIRY CARD

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rate generator or external modem. Switch-selectable rates of 45.5 to 9600 bits/s are derived from a crystal clock by the bit rate generator. There are also provisions for an external bit rate or alternate clock source.

Each of 16 address lines, eight data lines, and nine control lines are buffered and routed to a backplane distribution panel connector for expansion of the system with additional memory and 1/0 boards. All 1/0 devices are treated in the same manner as when executing a memory read or write instruction. The system can address up to 65k locations, of which 32k are allocated to RAM, 8k to EPROM, and the rest to I/O devices, utility boards, p/ROM programmer, and custom devices for special applications. Each plug-in expansion board has its own address decoding and will communicate with the processor only when addressed. All expansion boards have compatible connector pin assignments, permitting any board to be plugged into any slot in the card file.

Read/Write Memory

RAM expansion boards for the system are available with increments of either 1k x 8 static (up to 4k) or 4k x 8 dynamic (up to 16k). Systems will maintain multiple boards up to 32k or until card file locations are full. Assignment switches on each board determine the address area to which a particular board will respond.

Modem Channels

Modem boards for the system include 300-, 1200/1800-, and 2400-baud frequency shift key (FSK) configurations. In addition, 4800- and 9600-baud operation can be accomplished by attaching peripheral modems. Frequency division multiplex (FDM) boards can be included for 75-, 300-, and 600-baud requirements. FSK and FDM operations can be alone or simultaneous.

The ability to communicate with remote devices using either dedicated or switched telecommunications facilities is provided by modem and I/O port boards. A typical modem channel (diagram) operates at data rates of up to 1200 baud on a switched network or up to 1800 baud over dedicated facilities with C2 conditioning or better. Transformer coupled communications line inputs and outputs may be configured to

operate 4-wire full-duplex, as well as 2-wire half-duplex or simplex using an active hybrid.

An FSK technique is used with frequencies of 1200 and 2200 Hz representing mark and space, respectively, with data transmitted in the asynchronous format. To eliminate spurious noise encountered during carrier turnoff, the transmitter sends a 900-Hz soft carrier turnoff signal before squelching the transmitter, which activates a clamping circuit in the received remote modem. This forces the received data to the mark condition just prior to carrier turnoff. Transmit output levels are switch selectable for 0, -3, -6, or -9 dBminto a $600-\Omega$ load.

Received input signals within the receiver dynamic range of from -40 to 6 dBm are buffered and applied to a bandpass filter network which rejects out of band signals to improve noise rejection. The presence of a received carrier is detected only by the receipt of an incoming tone within the bandpass limits. Received carrier detection is used to squelch the receiver during carrier loss. Active filters discriminate between mark and space frequencies. The output is serial received data input to the system via its serial port.

The serial data port is very similar to that on the microprocessor board, but is used in the asynchronous mode only with internally generated bit rates of up to 1200 baud. External bit rate clock inputs of 16 or 64 times bit rate are provided, which are used for data rates between 1200 and 1800 baud. The modem and 1/0 port operate completely code transparent at 5, 6, 7, or 8 levels, with 1, 1.5, or 2 stop bits, and odd, even, or no parity.

Input/Output Ports

Single or multiple I/O port boards can be included in a system up to card file capacity. A dual serial I/O port board provides full duplex channels by incorporating two I/O data ports. Each channel can operate completely independent of the other with TTL, EIA RS-232-C, and 20-, 30-, or 60-mA current loop in neutral or polar I/O levels. The current loop I/O ports are optically isolated utilizing semiconductor switching. Loop battery and current loop regulators must be externally supplied.

Systems requiring multiple channels of serial I/O data can be expanded by including an 8-channel

board. Each channel is full duplex with TTL and EIA I/O levels.

Provision is made for up to four bit rate generators, one is basic and the other three are plug-in expansions. Each bit rate generator provides 15 switch-selectable rates plus an external TTL bit rate clock input. The four bit rate generator outputs are bused to all eight ports where DIP switches permit connection of any bus to the receive or transmit sections. For operation in the synchronous or isosynchronous modes, separate EIA RS-232-C level clock inputs are brought in for the transmit sections of each port.

Modem controls on each channel include request to send, clear to send, data set ready, and data terminal ready. The data set ready line is designed for general-purpose use and can be reassigned to monitor other modem status functions such as carrier detect or ring indicator.

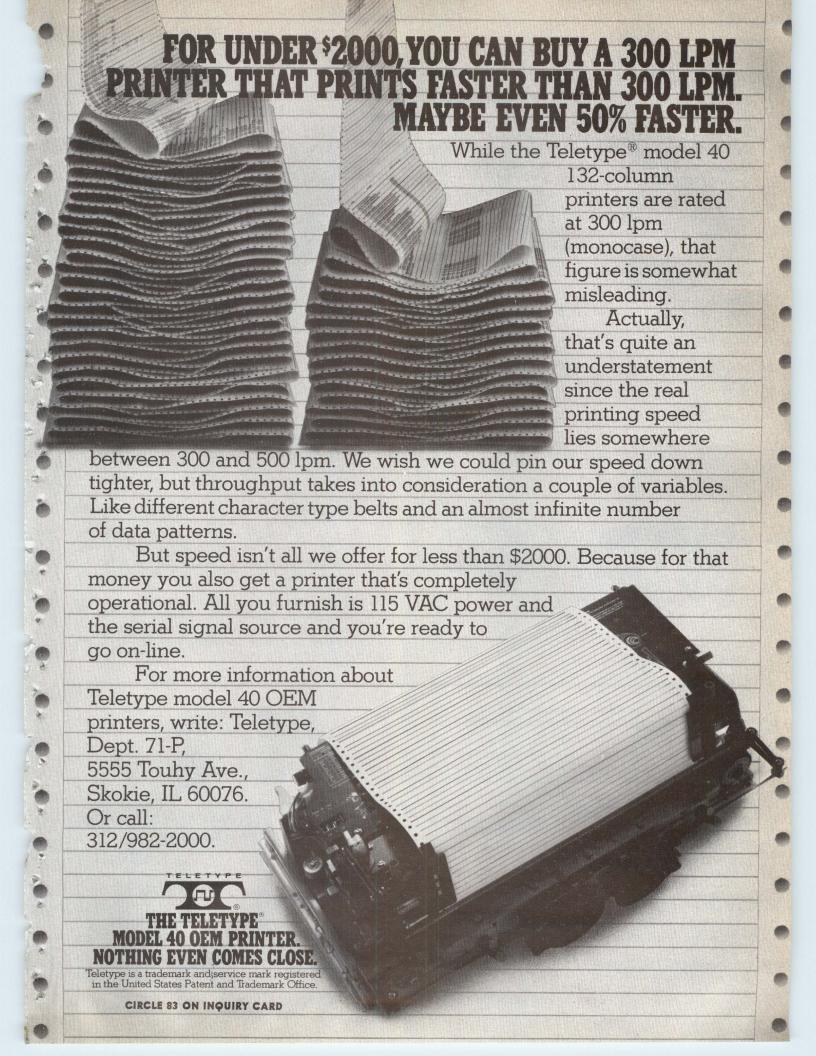
Parallel data transfer is enabled by a quad 16-bit parallel I/o port board. The four 16-bit lines can also be handled in 8-bit increments to a maximum of 64 bits. Each 8-bit group includes two handshake lines which can be configured by the control program to serve in a ready/ acknowledge sequence or as a data strobe.

The eight data bits can be used for inputs or outputs as determined by an 8-bit data direction register within the port, which is loaded by the microprocessor program. Outputs may be buffered with open collector drivers at TTL levels, or for actuation of relays and other devices up to 40 mA of current and a maximum of 30 V. When configured as inputs, the data lines accept TTL levels and are provided with resistor network termination.

Price and Delivery

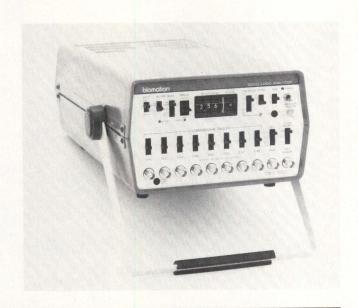
Single unit prices for basic Datamax 6 units including rack and microprocessor board are PRH-30, \$1400; PRH-32, \$1200; PRH-34, \$500; and DM-60, \$1100. Prices of various boards range from \$400 for the 4k memory to \$1000 for the 16k memory and 2400-baud modem. OEM discounts are available. Deliveries are three weeks ARO. Telcon Industries, Inc, 5701 NW 31st Ave, Ft Lauderdale, FL 33309. Tel: (305) 971-2250.

For additional information circle 199 on inquiry card.



9-Channel Logic Analyzer Adapts to Use As Engineering Or Troubleshooting Aid

Basically a 9-channel logic analyzer, the 920-D has outputs that allow display of the nine traces on virtually any oscilloscope or CRT display unit. Compact size, light weight, and low cost suit it to use by field service technicians. The ninth channel can be an extra signal input, a trigger marker and qualifier, or external clock qualifier. A latch input mode allows pulses or glitches as narrow as 10 ns to be captured. Input impedance is 1 $M\Omega$ and provision for use of X1 or X10 scope probes is built in. Fixed threshold levels for TTL and ECL and variable threshold voltages are available. The analyzer records in two distinct modes: delayed and pretrigger. Trigger delay may be specified in terms of clock periods up to a max of 9990 or trigger events may be specified as a delay quantity. The instrument accepts an external clock at any rate from dc to 20 MHz since the memory is a static RAM. Internal clock intervals are switch-selectable from 0.5 to 50 ms. Biomation Corp, 10411 Bubb Rd, Cupertino, CA 95014. Circle 200 on Inquiry Card



2400-Bit/s Modem Offers Fast Synchronization for Multistation Polled Networks



Circle 201 on Inquiry Card

Designed for 2400/1200-bit/s operation over 2- or 4-wire dedicated or dial networks, the 2400 LSI modem employs a 4-phase modulation technique conforming to CCITT type A or B and is online-compatible with Bell System 201B or C data sets, most other PSK modems, and the Bell 801 automatic calling unit. Strap options are provided for selecting transmitter output levels, carrier detect level, internal or external clock, carrier detector response time, RTC/CTS delays, and equalization. When operating over the DDD network, automatic answer circuits enable unattended call answering when connected via a type CBS or CBT data coupler. In autoanswer mode, an answer tone of 2025 Hz is generated for 3 s to switch 801 devices or alert manual calling stations of call completion. Built-in test pattern generator and receiver pattern detector simplify on- and offline testing and troubleshooting. Penril Corp, Data Communications Div, 5520 Randolph Rd, Rockville, MD 20852.

Power Supply Tester Performs Automatic High Volume Manufacturing/Incoming Inspection Tests

UTS-1900 integrates computer technology with analog loads and source potentials required for power supply testing. Capable of testing various power supply configurations with minor adaptations of the interface cable, it can be operated with a minimum of personnel training. The unit provides 1900 W of dc load capability distributed over six electrically isolated loads with 0.5% of full scale accuracy. Line input is provided by a loop-controlled autotransformer capable of 0 to 280 V rms at 20 A with ±1-V rms accuracy. Two programmable dc power supplies from 0 to 30 Vdc at 5 A are provided for dc-dc converter or special function testing. 16 measurement lines can be switched individually to a 51/2place DMM, for measuring volts ac and dc, and resistance in kilohms. A 31/2-place scanning measurement system, capable of 100 conversions/s, provides continuous load current, line voltage, and line current information which is displayed on the CRT screen during unit test. Autotest Co, PO Box 20264, San Antonio, TX 78220. Circle 202 on Inquiry Card





microNOVA keeps on trackin'.

Southern Railway has a long track record of being one of the most profitable rail systems in the country. To help stay on that track, they decided to increase the speed and flexibility of their online distributed communications network. So Southern Railway is now changing dumb terminals into intelligent ones throughout its rail system, using microNOVA microcomputers.

Southern Railway found that only the Data General microNOVA microcomputers could help them cut costs and keep track of some 75,000 freight cars moving over 10,500 miles of track, and do it the way Southern Railway wanted to. Controlling rolling inventory like that takes a lot of flexibility. And that's the big advantage Data General microNOVA microcompu-

ters bring to any application. Whether in a chip, on a board, or as a packaged system.

With the speed, flexibility and software of a minicomputer and the economies of microprocessor technology, microNOVA microcomputers let you do things your way. That's why they're setting track records in all kinds of applications.

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It's smart business.



With EPIC DATA'S new Model 1647 data collection terminals and Model 1648 system control units (SCUs), you can configure exactly the data collection system you need. These "building blocks," based on microprocessor architecture and modularity, allow you to provide your customers with simple, practical and flexible terminals or systems for virtually any combination of requirements they may have.

Simple. EPIC DATA terminals with RS232C interface (ASCII), or optional alternative interfaces, are simple to use and deploy. No computer knowledge is required. Data collection building blocks can be combined to enable collection of information from a wide variety of pre-prepared and variable data. Maximum use of pre-prepared data reduces entry errors.

All models include an 8080 microprocessor; the user can program terminals to provide customized input, output and processing of data. In addition, programmability aids in prompting the user through entry steps, validating data and enables off-line or on-line operation.

EPIC DATA terminals weigh only $8\frac{1}{2}$ pounds. They can hang on a wall, be placed on a desk, and are easily exchanged during maintenance.

Practical. EPIC DATA terminals are designed with permanence in mind. Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in a demonstrated MTBF of over 19,000 hours. MTTR is only 30 minutes.

flexible. Choose the terminal and options which best meet your application. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Terminals can be configured to scan bar codes and magnetic stripes or accommodate other peripherals through RS232 ports. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. A low-speed modem and serial asynchronous or synchronous communications ports with either RS232 or line driver I/O may be added. Both PROM and RAM memories are expandable.



SCUS. Model 1648 SCUs can be configured to poll up to 100 terminals, assemble transactions, format data, append time and date, and store or forward collected data to the host.

Let EPIC DATA show you how microprocessor-based architecture and building block modularity will provide you with simple, practical and flexible data collection terminals and SCUs.

OEM quantity (100) prices start at approximately \$1000. Contact your Epic Data representative today or write:

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How FORTHtm software tools have rescued mini and micro project developers reads like a fairy tale.

short time ago, a gloomy Monday found a New York manufacturer desperate. Microprocessor software problems had deep-sixed the delivery date of an artificial-kidney tester.

Four man-months of assembly language programming...and still the device wouldn't work.

Came Tuesday, design specs were rushed to a group of software problem-solvers, FORTH, Inc. Three nights a crack FORTH programmer concentrated on saving the day...flying cross-country to project headquarters on Friday.

By Sunday night, the machine was totally operational!

Five FORTH days, with one man applying microFORTH language and programming techniques, and the tough software task was fully written, debugged and cross-compiled.

For a complicated μP device with: one master panel with thumbwheels, 3-way switch, pushbuttons. Plus dual control panels with more thumbwheels, switches...and lights. Plus two printers; A/D converter; and hydraulic valves. All up in less than a week.

elieving in FORTH has solved many a minicomputer project too.

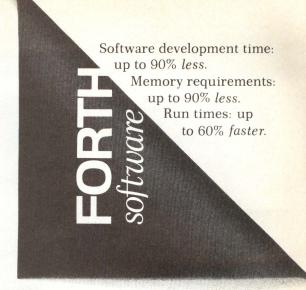
As when the Navy was caught between the devil and the deep blue sea. mini-hardware already configured to develop a missile guidance system required an image processing capability.

The hang-up? High level languages demanded too much memory; but assembler code, too much development time.

Fortunately, project management was wise to FORTH's track record in image processing. *And* the availability of off-the-shelf miniFORTH software that could accommodate just about any-make mini...on order, on hand, or on line.

National secrets can't be spilled, but what can be told is the performance of miniFORTH tools in the hands of *typical* users: software development time, 3-10 times less. Memory requirements reduced up to 50% over assembly code, with full machine speed capability. All simultaneously!

Easy to see why the Navy selected FORTH as the sole source for this software contract.



FORTH is fact...not fable. There is a popular myth: it says you can optimize today's advanced mini/micro hardware — with software tools as old as some programmers. But wishing won't make it so; you need rich new programming techniques.

That's FORTH. Combining the operating system with a multilevel language structure, you instruct machines on your own terms.

Whether you're talking new product development or on-going applications. All the way from process control to interactive graphics to data base management systems, FORTH helps you repeat these success stories. Either through our custom programming services. Or take FORTH tools off-the-shelf for in-house use.

For minicomputer projects, miniFORTH is ready to go for all popular minis.

microFORTH runs on disk-based microprocessor development systems, package-priced at \$2500, plus options.

So flexible, so powerful are FORTH capabilities, our case histories strain credulity. We admit it. And we admit, to learn this new shortcut, you'll leave the old-shoe comfort of Basic and Fortran behind.

It's worth it. In cost-effectiveness. In dramatic cuts in development time. In much lower computing-equipment investments. Just what it takes to make heroes in real life.



oral. You don't have to believe in fairy tales, to know that the limitations of Basic, PL/M, and Fortran are often pretty grim.

Calling FORTH in late can save your neck. But calling FORTH *first* can make any software project easier to swallow.

Phone (213) 372-8493, for microFORTH, miniFORTH or programming assistance. Or write: FORTH Inc., 815 Manhattan Avenue, Manhattan Beach, CA 90266. We can help.



CHARACTER-ORIENTED WORD PROCESSING SYSTEM

Char-oriented Electric Pencil software allows text to be entered and manipulated at any location as a continuous string of char. Lines, which are not delineated, are formatted automatically. Features include cursor controls, search commands, and scrolling. Four versions of software require min system hardware of 8080- or Z80-based microcomputer, 8k of memory, printer (Diablo Hy-Type II, TTY, etc), printer to computer interface, video display interface (VDM-1 or Polymorphic), video display monitor, Tarbell cassette interface, and cassette recorder. Michael Shrayer, 3901 Los Feliz Blvd, #210, Los Angeles, CA 90027

Circle 203 on Inquiry Card

RUGGEDIZED MINICOMPUTER



Comprised of two models—6/43 with a 32-bit access capability and 6/36 with 16-bit access—ruggedized level 6 systems are available in 13 x 17.5" (33 x 44.5-cm) assemblies, mountable on shock pads, flat surfaces, or std 19" (48-cm) wide racks. They operate from 120-V, 50- or 60-cycle outlets or can be adapted to 400-cycle aircraft power supplies. Filtering is added to meet emi/rfi and Tempest specs. RL6 meets MIL-E-5400 and -16400 stds. Honeywell Information Systems, 200 Smith St, Waltham, MA 02154. Circle 204 on Inquiry Card

DISC CONTROLLER

A terminal-resident, microprogrammed disc controller interfaces the HP 2645A-41A-49A intelligent terminal series with up to four Ampex DM 440 series disc drives to provide 40M bytes of online disc storage (10M bytes/drive). Heart of the 13 x 4" (33.02 x 10.16-cm) disc interface board is the model MSC-264X, featuring low power Schottky TTL and MSI functions. In addition to I/O commands, the controller has firmware diagnostic routines. Microcomputer Systems Corp, 440 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 205 on Inquiry Card

DUAL MINIFLOPPY SYSTEM KITS



Designed for use with the company's 6800 system, MF-68 minifloppy disc system includes all hardware and software. It can be expanded to its 4-drive limit with an expansion kit containing power supply, chassis, and two assembled minifloppy drives. Kit consists of controller, chassis, cover, power supply, interconnection cables, two assembled Shugart minifloppy drives, and diskette with FDOS operating system and disc BASIC software. **Southwest Technical Products Corp**, 219 W Rhapsody, San Antonio, TX 78216.

Circle 206 on Inquiry Card

PRINTED CIRCUIT EDGE CONNECTORS

Connectors allow as many as 85 PC contacts to be inserted in one operation. Contacts can be single- or double-sided with 0.1" (2.54-mm) and 0.156" (3.96-mm) spacings, providing up to 85 and 50 contacts on each side, respectively. Contacts are comprised of high tensile material and three gold-plating thicknesses—0.5, 0.76, and 1.2 μ m. Six mounting configurations are available. Each spacing version is available with five tail styles and four contact configurations. Amphenol Tyree Pty Ltd, 2875 S 25th Ave, Broadview, IL 60153. Circle 207 on Inquiry Card

OPTICAL TAPE READER



For use with microcomputer systems and terminals, 4031 is a bidirectional reader, with speed of 0 to 120 char/s asynchronous. With up to 60% transmissivity, it can be converted for 5-, 6-, 7-, and 8-channel tapes. Control electronics are on one board containing read head with light source connector for motor and connectors for I/O signals to the reader. It fits into a 2-module, 19" (48-cm) rack panel. Facit-Addo, Inc, 66 Field Point Rd, Greenwich, CT 06830.

PC CARD LOCKING DEVICE

For use in Versamount PC card brackets, Kard-Lok™ provides positive holding of the PC card into its connector against shock or vibration. A flat, stainless steel spring which is inserted into the bracket, the device is positioned to the height of the PC card and the toothedged section is pressed into the plastic channel of the bracket, making a permanent fastening. Boards from 4 to 7.5″ (10 to 19 cm) long can be locked in. Unitrack Div, Calabro Plastics, Inc, 8738 W Chester Pike, Upper Darby, PA 19082.

Circle 209 on Inquiry Card

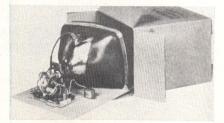
CARD READER FOR HOSTILE ENVIRONMENTS



Model 2972 has frontpanel lever that operates 864 switch functions to read std 80-col paper or plastic Hollerith punch cards. Interface options include diode-isolated matrix for Hollerith, numeric, alphanumeric (40- and 60-char sets), BCD, and special word length configurations. Normally closed contacts have gold-over-nickel plating with ratings of 0.25 A dc resistive in parallel and 0.50 A in serial with <50 m Ω contact resistance. AMP, Capitron Div, Elizabethtown, PA 17022. Circle 210 on Inquiry Card

FRAMELESS CRT DISPLAY

Supplied without frame or chassis, in both 9 and 12" (23- and 30-cm) sizes, TVX models are fully cabled, tested, and aligned, and ready to run. Components are mounted to a hardboard shipping plate, and interconnected with plug-in cables. Individual parts consist of CRT with yoke in place, flyback transformer, choke, and PC board. Units are identical to the company's TV series g-p monitors except for wire frame. Ball Corp, Electronic Display Div, PO Box 3376, St Paul, MN 55165.



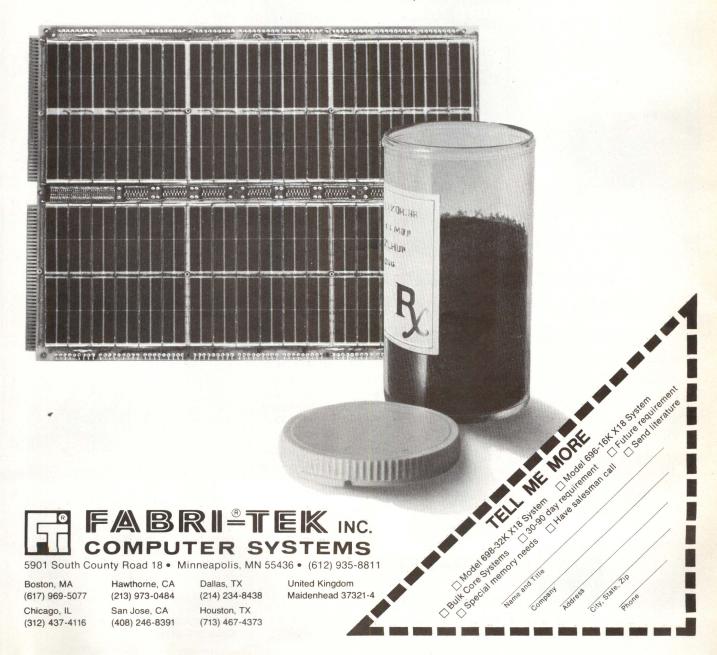
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Suffering from temporary loss of memory?

Try the Fabri-Tek core remedy.

If you're like some people who've been on a straight semiconductor memory diet, you've probably been experiencing severe complications. Loss of memory when power is removed. "Soft" random errors that can't be diagnosed. Temperature sensitivity. Added cost and complexity of error detection and correction schemes and battery back up.

For no added cost, core memories provide greater reliability, maintainability, non-volatility and 20 years of proven technology. They're relied upon in process control and a lot of other demanding applications where a failure could be catastrophic. Take our Model 698: 64K bytes of 650 nsec cycle time and 250 nsec access time. You can build a system up to 512K bytes. (Micro 3000 compatible, too). Maybe its time you kicked the semiconductor habit. We're ready to help.



DIGITAL POSITION ENCODER WITH ABSOLUTE OUTPUT



Econocoder^R rotary shaft encoder consists of miniature electromagnetic transducer and single PCB which can be located over 200' (60 m) away from motion being measured. Std output resolutions are 10 bits/360 deg in binary code, and 200, 360, 400, 1000 counts/360 deg of BCD formatted information. Output logic levels are DTL/TTL-compatible. Transducer has 1.5" (3.8 cm) dia, operates in temp range of 20 to 85°C, and has max slew speed of 3000 r/min. Starting torque is 0.1 oz-in (0.0007 N*m). Astrosystems, Inc, 6 Nevada Dr, Lake Success, NY 11040. Circle 212 on Inquiry Card

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LOW COST LIQUID CRYSTAL DISPLAY



A $3\frac{1}{2}$ -digit LCD, with an integral 1-chip CMOS LSI ADC, employs the field-effect method. The ADC consists of linear and digital CMOS, and includes oscillation and driving circuits for the LCD. Features include small size, low power consumption, and life of several hundreds of hours of continuous usage when the DMM or DPM is battery driven. Symbols of ac or — are displayed before the numerals; units of m, V, A, M, k, and Ω are displayed after them. **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505. Circle 213 on Inquiry Card

FLEXIBLE DISC DRIVE

Utilizing a band-driven design concept similar to IBM units, the low cost, high performance disc drive fits most mini or microcomputer applications. Series B82 random access drive offers up to 6.4M bits/disc for a single-density drive and up to 12.8M bits/disc, double-density. It stores up to 1.6M bytes on a std 8" (20-cm) diskette. MFM, M²FM, and GCR encoding techniques are used. Avg access is 91 ms with track-to-track access of 3 ms. **Micro Peripherals Inc**, 8724 Woodley, Sepulveda, CA 91343. Circle 214 on Inquiry Card

MINI/MICROCOMPUTER COMMUNICATION LINK



A portable, interactive terminal capable of interfacing to any mini/microcomputer via an RS-232 or current-loop port at selectable data transmission speeds from 110 to 9600 baud, CO-4420 consists of 1M-byte direct access tape drive, full ASCII keyboard, 40-char plasma display, RS-232 port, and microprocessor controller. Together in a compact case, they weigh only 23 lb (10.5 kg). LINCtape drive provides reliable mass storage. Computer Operations, Inc, 9700-B Palmer Hwy, Lanham, MD 20801.

Circle 215 on Inquiry Card

EPITAPE HOLDS THE RECORD FOR DATACOMM DIAGNOSTICS

EPITAPE holds the record — the record that greatly expands your ability to analyze data communications traffic.

EPITAPE is an effective datacomm analysis tool because it literally "duplicates the line." It captures full-duplex data dialog, in real time, at a switch selectable rate from 50 to 19,200 BPS. The data can be held for as long as you wish and then reconstructed — either at system speed or at a slower rate for detailed analysis. In either case, you have precise data, control status and regenerated clock

to reconstruct events as they actually occurred on the communications line.

The unit is independent of modem clocks and line disci-

plines, including async, bisync, SDLC and any others. Full-duplex data, along with six RS-232 control signals can be captured and replayed. External and manual event markers simplify subsequent location and retrieval of specific transactions which may be vital to solving your problem.

EPITAPE'S portability simplifies its application in widely dispersed systems; it weighs just 26 pounds and fits into a compact 5" x 20" x 17 1/2" package.

Be a record holder — use EPITAPE to reconstruct the line transmissions in

your data communications network. For details, contact Epicom, Inc., 592 North Douglas Ave., Altamonte Springs, Fl. 32701. Telephone 305/869-5000.



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SINGLE- AND TRIPLE-**OUTPUT SUPPLIES**

With a reduced size of 90 in3 (1474.8 cm3), DS series switching power supplies feature power outputs of 150 W and up to 80% efficiency for full power operation with min cooling. Two single output models are rated 5 V at 30 A, or 12 V at 12 A; all three triple output models offer 5 V at up to 24 A. Auxiliary outputs are ±12 or ±15 V at 3 A,



or 12 V at 4 A, -12 V at 1 A. Shortcircuit and overvoltage protection, and over temp "Guardian" circuit are std. Digital Power Corp, 2060 The Alameda, San Jose, CA 95126. Circle 216 on Inquiry Card

MILITARY/HI-REL ADC

ZAD3213, an ultra high performance, 13-bit ADC is capable of withstanding severe environments; it is designed, qualified, and screened to meet or exceed quality levels imposed by MIL-STD-883B. Fully encapsulated and sealed in a rugged metal case measuring 2.12 x 4.0 x 0.45" (5.38 x 10.16 x 1.14 cm), the device features conversion time of 100 μs max, differential nonlinearity of ±1/2 LSB max, and input range of 0 to 10 V. Output coding is unipolar binary. Op temp range is -25 to 100°C; storage temp is -55 to 125°C. Zeltex, Inc, 940 Detroit Ave, Concord, CA 94518. Circle 217 on Inquiry Card

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You Are Wasting More In Dollars For Human Resources Than This LINE PRINTER Costs

MODEL 8210 - \$3450* MODEL 8230 - \$3785*

2400 LPM - 80 COL. 1400 LPM - 132 COL



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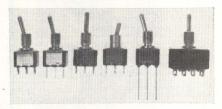
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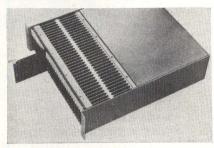
* Domestic USA Prices, Qty 1, End User

MINIATURE TOGGLE SWITCHES



Available in spdt, dpdt, 3pdt, and 4pdt models, the line of 24 switches includes bat handled and flatted toggle models. Wirewrap and PC board types feature gold plated terminals and contacts, and are rated at 0.4 VA at 20 V max, ac or dc. Solder terminal types have rating of 5 A with resistive load at 120 Vac or 28 Vdc. Raytheon Co, Distributor Products Operation, Fourth Ave, Burlington, MA 01803. Circle 218 on Inquiry Card

14M-BIT MEMORY IN RACKMOUNT CHASSIS



The 2601 14M-bit memory contains power supplies, forced air cooling, and cards for timing and control, address buffer, termination, and register. Contained in a single 5.25" (13.34-cm) high Retma rackmount chassis, the modular memory is designed around a 16k x 1 dynamic RAM. Bit lengths of memory array cards can be arranged to meet user requirements. Address, data input, and data output buses are arranged to permit addressing up to eight 768kword modules. Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110.

Circle 219 on Inquiry Card

The CRT terminal for the systems designer

You can change it to fit your system—instead of vice versa.

New microtechnology, new systems, new applications. It's all changing quickly. Our challenge: design a CRT terminal flexible enough to keep up with your ideas—one to help you make the most of your latest system, not compromise it. The 480/25 is the result.

Need an intelligent CRT terminal?

O.K. The 480/25 is an addressable/pollable intelligent CRT terminal that can accommodate a variety of protocols. It offers local editing, protected field formats, block transmission, and more.

It can save time; no time-fill characters needed, even at 9600 bits per second.

It offers cursor positioning by—and reporting to—the host computer.
And, of course, it can store forms locally and automatically check formats.

Need a cluster controller or a microcomputer?

Fine. One 480/25 can control a series of terminals and also communicate with a host computer. Or, you can add a disc, a printer, and expanded memory to a 480/25—and you've created a true microcomputer with integrated CRT and keyboard.

Etc., etc., etc.

The fact is, combine your software and the right peripherals and you can have 480/25 doing all kinds of handsprings for you. So instead of clamping a lid on your system, it can spring loose some great ideas.

Get the details.

It's easy, just ask.
Call (213) 966-3511. Or write.
CONRAC, 600 N. Rimsdale Avenue,
Covina, CA 91722



CONRAC

PDP-11 COMPATIBLE CLUSTER TERMINAL CONTROLLER

CVD-11 allows the PDP-11 to handle up to 32 remote CRT stations. Consisting of a controller card that plugs into hex slot and two remote interfaces, the card contains all electronics to support two CRT stations, including independent display memories, char generators, TV sync generator, and Unibus[®] interface. Features include a



video/data multiplexer which allows keyboard, printer, and TV monitor to share a single coax wire. ECHOlab, Inc, 213 Middlesex Tpk, Burlington, MA 01803.

Circle 220 on Inquiry Card

MICROPROCESSOR TEST SYSTEM

MT-17 provides testing in a conditioned natural environment in which logic sequence, through which the DUT is exercised, is written in the language of the microprocessor. User has full programmable control over all test variables including logic levels, bias voltages, timing edge placement, and formatting of data, addresses, and clocks. Operating modes include go/ no-go testing and sorting into bins. Adar Associates, 11B North Ave, Burlington, MA 01803.

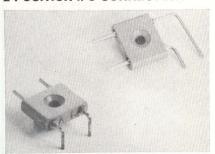
Circle 221 on Inquiry Card

ALPHANUMERIC IMPACT PRINTERS



Measuring 2.3 x 5.8 x 6.0" (5.84 x 14.73 x 15.24 cm), series PR2100 prints at speeds up to 3.0 lines/s for numeric and 1.5 lines/s for full alphanumeric. Spanning hammers form characters for each group of three columns. Start-up time of 750 ms and paper slewing of up to 10 lines/s are featured. Power consumption of the drive motor is 3 W. Std options include special drums, vertical mounting, single line slip validation, and special voltages. Sheldon-Sodeco Printer Corp, 4 Westchester Plaza, Elmsford, NY 10523. Circle 222 on Inquiry Card

2-POSITION I/O CONNECTORS



GFPL series connectors (available with mixed or nonmixed gender) mount horizontally or vertically to a circuit board or panel. Narrow width and countersunk mounting hole permits flat, secure counting. Any number may be ganged on a rod or bolt to obtain custom multicontact connectors, with or without a variety of positive polarization configurations. Molded in diallyl phthalate, the connectors have gold-plated contacts. Positronic Industries, Inc, PO Box H, 208 W Center St, Rogersville, MO 65742. Circle 223 on Inquiry Card



Zeta Research A Division of Nicolet Instrument Corporation



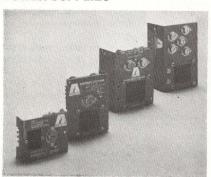
for all Zeta on-line plotters -

FIXED-HEAD DISC DRIVE CONTROLLERS

Available in configurations transparent to either DEC's RK05, RF11, or RC11 controllers, the DC-111 enables discs to operate in rugged environments. Up to eight 980 fixed-head disc drives may be daisy-chained and run through a single controller, providing up to 16M bytes of continuous storage. It is also transparent to RSX-11 or RS-64 operating systems, and is fully compatible with Unibus^R. Packaged on three DECtype quad boards, the device is mounted as a 4-slot system unit. Dataflux Corp, 1195 E Arques Ave, Sunnyvale, CA 94086.

Circle 224 on Inquiry Card

OPEN FRAME POWER SUPPLIES



With inputs of 100 to 125 or 200 to 250 Vac over a 47- to 440-Hz range, 55 models of the ALM series provide full, nonderated performance at 50-Hz operation. Regulation is specified at 0.1% (line and load), with ripple and noise rated at 1.5 mV rms, 5 mV pk-pk, over a 47- to 63-Hz range. Single output models range from 2-V units providing 1.5 to 20 A at 40°C through 24-V units providing 0.5 to 10.5 A. Dual output models with adj output range of 11.8 to 15.2 V have current ratings of 0.55 to 8.0 A. Acme Electric Corp, Cuba, NY 14727.

Circle 225 on Inquiry Card

it in digital refresh memory, model CD5506 is suited for use with microscopic/telescopic images, and photo analysis. CD5508 digitizes an image to 256 grey levels. Optional intensity transformation table with 256 20-bit words allows simultaneous gamma-corrected grey scale/pseudocolor images to be displayed at same time. System interfaces to PDP-11 Unibus^R; other interfaces are optional. DeAnza Systems, Inc, 3444 De La Cruz Blvd, Santa Clara, CA 95050. Circle 226 on Inquiry Card

VIDEO DIGITIZER AND DISPLAY



Capable of capturing an image with 64 levels of grey scale and 512 x 512 pixel resolution in 0.033 s and storing

PROGRAMMABLE SOLID-STATE SWITCHES

With accuracies up to ±0.1 deg. switches have built-in absolute encoder with memory. Programming is via frontpanel-mounted thumbwheel switches which can be reprogrammed during operation. Outputs are digital logic levels, open collector transistors, or relays. Digital BCD or binary data, and dc outputs are available with 3- or 4digit LED display. Op temp range is 0 to 70°C or -55 to 85°C. Either 19 x 12 x 8.75" (48.26 x 28.48 x 22.22-cm) rack mount or 12 x 16 x 8" (28.48 x 40.64 x 20.32-cm) wall mount panel packaging is available. Computer Conversions Corp, 6 Dunton Ct, East Northport, NY 11731.

Circle 227 on Inquiry Card

Need a DEC Floppy System?

MF-11



The MicroFlop-11 is Your PDP-11V03 . . . in Half the Space . . . and at Half the Price.

Functionally identical to the PDP-11V03, and using only 10-1/2" rack space, the MF-11 houses the Shugart dual floppy system, the backplane for the LSI-11 with associated peripherals, and all needed power . . . at considerable dollar savings.

- Compact Version of PDP-11V03
- **Totally Software Compatible**
- RT-11 Fortran IV Basic
- Bootstrap Loader
- Optional Double Sided Drive
- Optional Extended Backplane
- 3740 Format

FD-1



Our FD-11 Dual Floppy System Does Everything DEC's RX-11 Will Do . . . and a Few Things More . . for a Lot Less.

FD-11 Dual Floppy Disk system with its Controller/ interface card offers you total software, hardware and media compatibility for all DEC PDP-11 and LSI-11 systems . . . and in addition:

- Over 35% Price Savings
- 8080 Based Controller
- **Industry Standard Drives**
- Write Protect Switches
- Unit Select Switches Bootstrap Loader
- Formatter and Self-test Routine
- Optional Double Sided Drives

For more details and pricing, contact: Marketing Department

UNIT PRICE

\$3440.00

\$4290.00

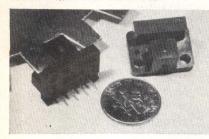
with LSI-11

Charles River Data Systems, Inc., 235 Bear Hill Rd., Waltham, MA 02154, Tel. (617) 890-1700

UNIT PRICE

\$2750.00

MINIATURE SOLID-STATE VANE POSITION SENSORS



Containing a std 0.04" (0.10-cm) sq Hall-effect IC chip on one side and a magnet on the other, the 0.75" (10.9 mm) long models 3AV/4AV can function from 0 to 100k operations/s, unaffected by dirt or ambient light. They may be interfaced directly with transistors, microprocessors, integrated logic, and SCRs. 8- and 20-mA outputs eliminate need for amplifiers. Both utilize supply voltage of 4.5 to 5.5 Vdc; 4AV also has versions using 6 to 16 Vdc. 3AV has an op temp range of 0 to 50°C; 4AV has a -40 to 85°C range. Micro Switch, div of Honeywell, 11 W Spring St, Freeport, IL 61032.

Circle 228 on Inquiry Card

ALPHANUMERIC DISPLAY SUBSYSTEMS

Argus alphanumeric display subsystems utilize dot matrix message panels (dcexcited plasma) to provide a 5 x 7 dot matrix char display format with std underline and cursor capability. The family of 14 subsystems consists of Mini or Maxi series which differ according to char sizes [0.21, 0.25, and 0.33" (0.53, 0.64, and 0.84 cm)], and overall size, weight, and power consumption. Char capacities are 32, 64, 128, and 256. Industrial Electronic Engineers, Inc. 7720-40 Lemona Ave, Van Nuys, CA 91405.

Circle 229 on Inquiry Card

BASE STATION TESTER FOR REMOTE LINES

The 68 Loopback Card operates in conjunction with the company's 6850 and 6385 FSK tone equipment to loopback digital interface or communications line at a remote location. Supervision of loopback functions is accomplished at the master station by manual switching or simple computer control. In line loopback mode for testing 4-wire communications facilities, the line is looped at the remote; in data loopback mode, received data and transmit data functions are connected. RFL Industries, Inc, Boonton, NJ 07005. Circle 230 on Inquiry Card

LINEAR OPTICAL ENCODERS



Two linear optical encoder series in modular and enclosed versions are available for digital velocity and displacement information. They consist of a photohead containing light source and detector, and a flat glass scale with photo-etched chrome pulse marks. The enclosed series is self-contained with its own set of linear bearings. Std lengths are from 10 to 36" (25 to 91 cm). The modular series mounts directly onto linear motion assemblies. Both offer linear velocity of 0 to 100" (0 to 254 cm)/s. Disc Instruments, Inc, 102 E Baker St, Costa Mesa, CA 92626. Circle 231 on Inquiry Card

LOW COST DELAY LINE

A 14-pin delay line series in a low profile DIP contains 15 models with inline or criss-cross termination. Total delay times range from 10 to 500 ns, impedance level is 100 Ω , and rise times range from 2.4 to 100 ns. Dc resistance of 1 Ω for the 10-ns delay line scales upward to 17 Ω for the 500-ns line. Tempco of delay is 120 ppm/°C over the op temp range of -55 to 125°C. Pulse Engineering Inc, PO Box 12235, San Diego, CA 92112. Circle 232 on Inquiry Card

ROYTRON plug-compatible reader/punch

Desktop combination reader/punch with serial asynchronous RS-232C compatible interface. Designed to operate with a terminal device on the same serial data lines or alone on a dedicated serial line. Reader will generate data at all standard baud rates up to 2400 baud.

Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batch, utilizing a 32 character buffer.

Two modes of operation are provided: Auto Mode - Simulates Model ASR 33 Teletype using ASCII defined data codes (DC 1, 2, 3 and 4) to activate/deactivate the reader or punch: Manual Mode - Code transparent mode. Panel switches control activation/deactivation of reader or punch and associated terminal device.

Tape duplication feature is provided by setting unit to LOCAL mode.



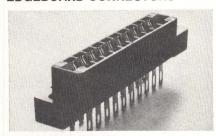
self-contained electronics and power supply. Complete in attractive noise dampening housing.

For full details, write or call us.

SWEDA INTERNATIONAL, INC. Litton O.E.M. Products

34 Maple Avenue, Pine Brook, N.J. 07058/(201) 575-8100 IN U.K. - ADLER BUS. SYSTEMS/OEM PRODS., Airport House, Purley Way, Croyden, Surrey, England IN FRANCE - SWEDA INTERNATIONAL/OEM, 103-107 Rue de Tocqueville, 75017 Paris, France

EDGEBOARD CONNECTORS



Designated the H41 series, the 0.156 x 0.200" (0.446 x 0.508-cm) grid device is designed to meet or exceed MIL-C-21097 performance stds. Contacts made of copper-nickel-tin alloy (CA 725) are bifurcated for connection redundancy. It is available with solder tail and eye terminations and from 10 to 25 contact positions. Interchangeable with most 1piece edgeboard connectors, the device achieves reliable electrical connections by preloading cantilever contacts for optimum normal force. Texas Instruments, Inc, Metallurgical Materials Div, 34 Forest St, Attleboro, MA 02703. Circle 233 on Inquiry Card

MINIATURE PCB POWER RELAY

Rated to switch up to 8 A at 240 Vac, type G2L relays are packaged in low profile configuration for use with PC boards rackmounted on 0.5" (1.27-cm) centers, or upright where PC boards have sufficient overhead clearance. Dimensions when low profile mounted are 0.413 x 1.004 x 1.122" (1.049 x 2.550 x 2.849 cm). Vertically mounted, height is 1.004" (2.550 cm) and base area is 0.413 x 1.122" (1.049 x 2.849 cm). Six coil voltages ranging from 3 to 48 Vdc are available. Typ power consumption in continuous operation is <520 mW. Operate time is 6 ms max and release time is 4 ms max. Mechanical service life is rated at 200M operations min. Omron Electronics, Inc, Sears Tower, 233 S Wacker Dr, Chicago, IL 60606.

Circle 234 on Inquiry Card

DIGITAL/ANALOG TEST SYSTEM



A computer-controlled system for testing and troubleshooting PC boards, electronic subassemblies, and complete assemblies, the 1796 is capable of both static and dynamic functional tests of digital, analog, or hybrid circuits. A high speed controller with dedicated memory for each driver/sensor pin provides the rates necessary to test dynamic logic, which requires high rate data I/O. Features include bidirectional bus testing at high speed, flexible synchronization, and digital I/O electronics that can switch from drive to sense at high speed while synchronizing with the UUT. Digital I/O operates through a universal scanner that allows digital and analog source and measure capability at each I/O pin. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742. Circle 235 on Inquiry Card

DESKTOP, SELF-CONTAINED COMPUTER SYSTEM

MCS-PT, complete with display and disc storage, full keyboard, and 12-slot motherboard, may be used either as a standalone processor or as a processor terminal in a larger



system. Features include a 15" (38-cm) high-resolution monitor; u/Ic ASCII keyboard with eight user-designated special function keys and 16-key numeric cluster pad; and Shugart SA-400 minifloppy disc drive. The 12-slot mainframe contains a CPU board with 8080 processor and a

special circuit that implements a start up "jump to" routine to any user-selected byte address 16k of RAM is provided; additional RAM is optional. The disc controller handles four drives; an I/O board provides three parallel and three serial ports with selectable baud rates of 75 to 19,200. **TEI, Inc,** 5636 Etheridge St, Houston, TX 77017.

Which Major Navy **Programs Specify** Librascope's Mass Memory Subsystem? TRIDENT (IR2) TACINTEL **SURTASS BQR-24** New one megaword Mass Memory Subsystem for TACINTEL features shock isolation and EMI/RFI secure packaging for mounting in an open standard 19" rack.

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The militarized Mass Memory Subsystems will meet the environmental specifications of MIL-E-16400 and MIL-E-5400 including MIL-S-901C, the drop hammer shock test.

Interface is provided for computers such as the $AN/UYK\ 7$, 15 and 20 with NTDS fast I/O, and for the Rolm militarized computers.

For complete information call (213) 244-6541 or write to Librascope Division of the Singer Company, 833 Sonora Avenue, Glendale, California 91201.







Save engineering time and expense. Take advantage of Intermec's years of expertise. The Intermec Model 9200 is a completely designed bar code reader that's ready to integrate into your system. All the programming needed is on the card. Read the code of your choice; Code 39, Codabar, UPC or another popular bar code. The reliable RUBY WAND® Light Pen is included in the low, low price of under \$400 in OEM quantities.

Features you'll get include bidirectional scanning, ASCII code transmission, and RS-232-C interface with dual connectors for operation with other devices. Parallel data interface boards and custom communications protocol are available or can be developed to meet your exact requirements.

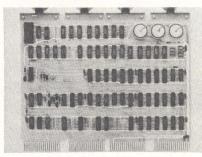
For more information, write or call: Interface Mechanisms, Inc. 5503-232nd St. S.W. Mountlake Terrace, WA 98043 Phone (206) 774-3511

PRODUCTS

HEAD PER TRACK DISC MASS MEMORY

Model Eighty has max capacity of 64M bits (8M bytes) and avg access time of 8.5 ms. A patented, fail-safe, retractable head design and a metal-plated disc sealed in a head chamber eliminate possibility of internally generated contamination from oxide-coated discs, or entrance of external contamination from an air intake. The unit is compatible with all of the company's controllers for Data General and DEC computers. Changing one interface card permits emulation of other manufacturers' products. Alpha Data Inc, 20750 Marilla St, Chatsworth, CA 91311. Circle 237 on Inquiry Card

TIME/DATE UNITS FOR PDP/LSI-11

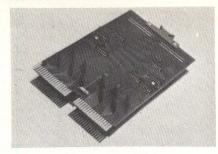


Presenting date and time upon simple read instruction, TCU-100 (timing control unit) for the PDP-11 can be set to interrupt at preset times, or regular intervals as short as 0.488 ms. It allows user to keep track of system downtime even during power failures. For the LSI-11, TCU-50 has the same features except interrupt capability. Both can operate for up to three months without power on built-in rechargeable batteries. Each unit is contained on an edgeconnector circuit board which plugs directly into computer's accessory slot. Digital Pathways, Inc, 4151 Middle-field Rd, Palo Alto, CA 94306. Circle 238 on Inquiry Card

RIBBON CABLE WIRING HARNESS

Latch wiring harnesses are available for connecting flat cable with DIP header plugs, receptacle, card edge, and paddle board plug connectors. Contacts are fully gold plated or gold plated on mating end and pre-tinned on displacement contact. Connector housings are made of UL-recognized 94 V-O rated material. Low cost, ribbon cable connectors are preassembled. AMP Special Industries, div of AMP Products Corp, Valley Forge, PA 19482. Circle 239 on Inquiry Card

BUS REPEATER FOR PDP-11 SYSTEMS



Allowing for physical and electrical extension of Unibus^R, OSB11-A bus repeater drives up to 19 extra bus loads or up to 50' (15.24-m) extra bus cable length. Compatible with DEC's DB11-A repeater, it is four times faster in Master Sync to return Slave Sync with a response time through the repeater of 80 ns max. It has 34 operational circuit components and requires no extra system unit. Any signal delay through repeater is 40 ns max. Datafusion Corp, 21031 Ventura Blvd, Woodland Hills, CA 91364. Circle 240 on Inquiry Card

SINGLE- AND **MULTIPLE-OUTPUT SUPPLIES**

Drop-in electrical and mechanical replacements for ACDC's OEM series power supplies are available in 78 single- and multiple-output models with nominal voltage ratings of 5 to 32 V, current ratings from 1.0 to 35 A, and max power of 277 W. Most models are UL 478 recognized—file number E47894A. Other features include a heavy duty barrier block for I/O connections, remote sensing, and programming capabilities. Deltron, Inc, Wissahickon Ave, North Wales, PA 19454. Circle 241 on Inquiry Card

PDP/LSI-11 ADD-IN MEMORY



Providing 8k, 16k, 24k, or 32k of memory on a single card, LS-IN-11 uses 8k or 16k dynamic MOS n-channel chips. Memory is completely hardware and software compatible with the DEC PDP-11/03 and with LSI-11 microcomputers. Memory segments are switch selectable from 0 to 32k, in 4k increments. Complete system plugs into single chassis slot position. Card size is 8.5 x 5.187 x 0.375" (21.59 x 13.17 x 0.95 cm). Fabri-Tek, Inc, 5901 S County Rd 18, Minneapolis, MN 55436.

Circle 242 on Inquiry Card

TAPE PERFORATORS

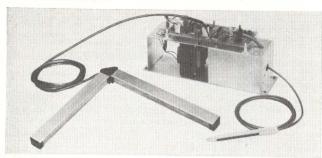
Series 6075 perforators have a punch speed of 75 char/s, which when combined with direct solenoid tape punching, dc motor drive, and sprocket feed, results in exceptional service life. The punch mechanism is estimated to maintain



its longitudinal registration for 25M char. Four models, each a self-contained rack-mounted unit with controls and power supply, are available. RPS6075 and RAB6075 are perforator-only and perforator/reader configurations for roll tape;

RPF6075 and RAF6075 are equivalent models for fanfold tape. The reader mechanism operates asynchronously at up to 300 char/s or continuously at faster rates. **Ex-Cell-O Corp, Remex Div,** 1733 Alton St, Irvine, CA 92713. Circle 243 on Inquiry Card

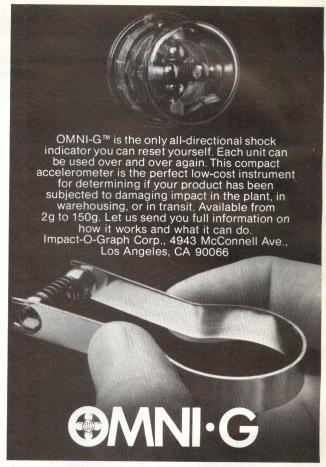
SONIC DIGITIZER



GP-101 consists of stylus, with or without ink, or cursor, electronics package, and sensor L-frame. Two sensors are mounted in a rigid, aluminum L-frame which can vary in length up to 60" (152 cm). This sensor assembly can be moved from tablet to CRT, projection screen, map table, or blackboard without recalibration or realignment of its true right angle. Output is in the form of two gating signals which are true from the time that the supersonic pulse is generated by the stylus or cursor until it reaches each of the sensors. The user must provide power supply circuitry, pulse timing and triggering circuitry, circuitry for converting the gate signals, and additional output or analysis circuitry. Science Accessories Corp, 970 Kings Hwy W, Southport, CT 06490. Circle 244 on Inquiry Card

REMOTE DATA ACQUISITION SYSTEM INTERFACE OPTIONS

An RS-232-C interface with switch-selectable baud rate gives the Micromux system complete ASCII serial communications capability and the power to interface with intelligent peripherals as well as micro- and minicomputers, and mainframes. Baud rates are 110, 150, 300, 600, 1200, or 2400. 2- and 4-wire, 20-mA current loop operation remains available. An RS-232-C clear to send feature allows computers to take data from the acquisition system in character or block increments. Located in the MM6100 receiver, the option transmits a std ASCII word. Up to seven MM6000 receivers (20-mA current loop) can be multidropped from one MM6100 receiver, allowing the user to operate a 512-channel system at low equipment cost. **Burr-Brown**, International Airport Industrial Pk, Tucson, AZ 85734.



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The wide variety of Instrument Specialties beryllium copper contact strips and contact rings in many sizes and shapes can help you solve your shielding and grounding problems. Standard catalog items work for most applications, but special adaptations are easily made and provide you with virtually a custom-designed part with only a one-time extra charge.

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PRODUCTS

SWITCHING REGULATORS

High frequency switching regulators, measuring 6.5 x 4.5 x 1.5" (16.5 x 11.4 x 3.8 cm), and weighing 1.7 lb (0.8 kg), are available in 5 Vdc at 10 and 20 A and \pm 12 Vdc, \pm 15 Vdc at 1.5 A configurations. Efficiency is \geq 75% at 5-V output and full load with nominal input line voltage (115 or 230 Vac.) Devices are convection cooled, have low ripple (PARD), are short-circuit proof, and have fast load transient recovery. Sola Electric, 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 246 on Inquiry Card

MINIATURE PANEL COUNTER

Designed for warranty recording, metering, and message registering applications, series 7286 electric counter is capable of 12- or 24-Vdc operation. Electrical impulses are recorded at up to 600 counts/min through temp range of 0 to 40°C. Power may be applied continuously. Max consumption is 2.5 W. Models with six or seven white on black figures fit a 1.630 x 1.140" (41.40 x 28.96-mm) panel cutout. **Veeder-Root**, Hartford, CT 06102. Circle 247 on Inquiry Card

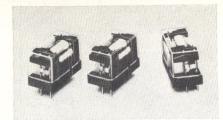
PDP-11 COMPATIBLE MAG TAPE CONTROLLER

TFC 802, an imbedded controller for PDP-11 Unibus[®] computers, offers both NRZI and/or phase-encoded recording techniques for std drives over speed range of 12.5" (31.75 cm) through 125" (317.5 cm)/s. Package consists of three boards in system unit with interconnecting cables to Unibus and tape drive. Units are compatible with DEC's RSX-11, RT-11, and DOS operating systems. Complete diagnostic software is supplied. **Aviv Corp**, 300 Sweetwater Ave, Bedford, MA 01730. Circle 248 on Inquiry Card

PRECISION BIFET OP AMPS

Two precision high speed op amps, models OP-16 and -17 feature min slew rates of 25 and 45 V/ μ s, and settling times of 700 and 400 ns to 0.1%, respectively. Containing a compensation circuit to maintain low input bias current at elevated temp, both devices have 500- μ V max input offset voltage, 5- μ V/°C max input offset voltage drift, and 11-nA max input bias currents. Both can be nulled; however, low offset voltage and drift can be provided without nulling. **Precision Monolithics, Inc,** 1500 Space Park Dr, Santa Clara, CA 95050. Circle 249 on Inquiry Card

FLUX TIGHT SUBMINIATURE PC RELAYS

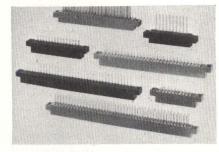


HA series relays achieve long life and high reliability through simple mechanism (only nine piece-parts), and manufacturing and packaging techniques used for molded construction. Initial contact resistance is 100 m Ω ; resistive load ratings are 750-VA, 90-W max switching power; 250-Vac, 30-Vdc max switching voltage; and 3-A max switching current. Expected life is 10M mechanical operations. Arrow-M Corp, 250 Sheffield St, Mountainside, NJ 07092. Circle 250 on Inquiry Card

MULTIPLE-OUTPUT HIGH VOLTAGE SUPPLY

Model 4000-1592 dynamic focus power supply offers economical, high performance for a range of commercial and military applications requiring a well-regulated source of high voltage for CRTs. The unit provides anode output to 15 kV, variable focus output of 2.2 to 2.4 kV, G-1 output of -10 to -50 V, and G-2 output of 300 V. Qualified to ground-based Mil Spec requirements, the device's focus output can be modulated over 0 to 400 V range. CPS, Inc, 722 E Evelyn Ave, Sunnyvale, CA 94086. Circle 251 on Inquiry Card

EDGE CONNECTORS



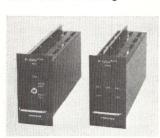
Edge connectors with 0.156" (0.396-cm) std spacing are available with 10 to 50 positions for single- or double-sided PCBs from 1.4 to 1.8 mm thick. Preloaded and bifurcated springs provide constant mechanical pressure on the board and two independent electrical contact areas for each circuit. Devices are available with gold flash or selective gold plating. The S-400 series is available in different mounting configurations and with eight terminal types. SMK Electronics Corp of America, 118 E Savarona Way, Carson, CA 90746. Circle 252 on Inquiry Card

BLOCK FLOATING-POINT-ARRAY SIGNAL PROCESSOR

MSP-5 is a single 15 x 15" (38 x 38-cm) plug-in board which is capable of performing 1024-point real fast Fourier transforms in under 7 ms when used in Interdata model 8/32 and 7/32 minicomputers. Requiring 5 V at 7.5 A, the board derives dc power from the host computer. The signal processor performs only the operation defined in its array library, which can be executed either by FORTRAN subroutine calls or by straightforward use of the host computer I/O instructions under assembly language. All boards are p/ROM driven but can be reprogrammed to accommodate a change of application. Input data arrays reside in host computer memory and are read and operated upon by the processor. Computer Design and Applications, Inc, 375 Elliot, Newton, MA 02159.

2-WIRE, FULL-DUPLEX, CONVERSATIONAL MODE 1200-BAUD MODEM

P-1200-Plus, a buffered version of the company's 1200/150 modem, is intended as a cost-effective alternative to the Vadic 3400. Buffering allows simulated 1200-baud full-duplex



transmission over dial-up or 2-wire leased lines; the unit interfaces with KSR-type data entry keyboards in an echoplex environment. Available in both answer and originate versions, the modem operates full- or half-duplex in any system interfaced with manual or automatic DAA. It connects with std EIA RS-232

or Teletype^R adapter and requires power of 115 Vac $\pm 20\%$; 60 Hz 5%; 7 W/channel over an operating temp range of 40 to 140°F (4 to 60°C). Bell System 113 series disconnect options are std. **Prentice Corp**, 795 San Antonio Rd, Palo Alto, CA 94303.

Circle 254 on Inquiry Card

GROUND FAULT RELAY SYSTEM

Adjustable for both current sensitivity and time delay, the GRC-100 can be set, at seven discrete steps, from 100 to 1200 A and at six separate time delays, from instantaneous to 0.5 s, allowing flexibility in coordinating with other ground



relays for proper tripping sequence. A flush-mounted optional accessory to the surface-mounted relay, the TMC test and monitor panel provides pilot light, target, and test which allow quick determination of

system status and a means for testing the circuit without interrupting service. The monitor's magnetic target shows if the relay has tripped and the pilot light indicates that control power is available to actuate the breaker. The target will maintain the correct indication even if control power is removed upon the opening of the disconnect means. Gould Inc, Switchgear Div, 501 Office Ctr Dr, Fort Washington, PA 19034.

Circle 255 on Inquiry Card



Magtape in Microprocessor size

Wafers are smaller than other magnetic tape packages. Less expensive too. So are MicroVox drives. That's why they go so well with microprocessors. Big performance, small size, low cost. A 50-foot Wafer is certified for 1.5 million flux changes. That's 1.5 megabits of MFM, 0.75 megabit of biphase or 0.5 megabit of ratio recording. Just right for loading your MPU. The price is right too. Wafers go for \$1.80 to \$4. Drives are \$36 to \$115. At those prices an MPU can afford to get loaded often.



MICRO COMMUNICATIONS CORP.

80 BACON STREET WALTHAM, MASS. 02154 617/899-8111

CIRCLE 98 ON INQUIRY CARD



A quality stepper motor and IC driver that cuts design costs, simplifies circuitry, minimizes space

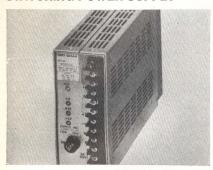
We've just put the cost of an incremental drive stepping system within reach! And we've simplified your job in doing so. The \$12.60 includes our K82701-P2 12V dc stepper motor and our SAA1027 IC driver in 100 piece quantities, basically all you need for a complete system, if you supply dc voltage and stepping pulse. The motor has a 7½° step angle, 200 steps/sec pull-in rate and 6.0 oz-in working torque. If these specs don't suit your proposed application, we have 7 other motors to choose from with pull-in rates and working torque values to satisfy most drive applications. 15° step angles are also available, as are 5V dc models. Any one of the 7 can be driven by the IC driver without the need for discrete power stages. Use of the driver, in fact, cuts the cost and complexity of your circuitry to the bone. It's small in size, low in cost and assures maximum stepping accuracy in conjunction with our stepper motors. Find out more about NAPCC stepper systems.

Write for information today!

NORTH AMERICAN PHILIPS CONTROLS CORP.

Cheshire, Conn. 06410 • (203) 272-0301

TRIPLE-OUTPUT SWITCHING POWER SUPPLY



RMT series features three outputs which are all stabilized in high efficiency switching mode. Principal output is 5 V at 10 A, with available auxiliary voltages of ±12; ±15; 12, -5; 15, -5; 12, -9 V, all rated at 1 A. All outputs are adjustable with built-in current limiters and overvoltage protection; the 5-V, 10-A output has remote error sensing. The 2.187 x 5.125 x 8.812" (5.554 x 13.0175 x 22.382-cm) units are enclosed, shielded, and filtered for emi suppression. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352. Circle 256 on Inquiry Card

QPL-APPROVED SOLID-STATE RELAYS

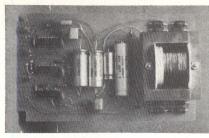
The JM640 series of solid-state relays are claimed as the first to receive QPL approval to MIL-R-28750, the military spec covering SSRs. Hermetically sealed in a TO-5 package specifically designed for military and aerospace applications, the relays include JM640-1, 643-1, and 643-2, qualified to MIL-R-28750/5, /6, and /7, respectively. Output ratings are 60 mA/40 V (dc or ac), 300 mA/40 Vdc, and 100 mA/250 Vdc, respectively. **Teledyne Relays**, 3155 W El Segundo Blvd, Hawthorne, CA 90250.

Circle 257 on Inquiry Card

SOCKET ASSEMBLIES FOR 10-A RELAYS

For 2- and 4-pole miniature, 10-A rated plug-in relays, 622BS and 624BS assemblies are designed to mount via Snaptrack[™] mounting channel in lengths to 4 ft (1.2 m). Individual assemblies feature #6-32 terminal screws with captive wire-clamp plates, breakresistant barriers, screws in the readyto-wire position, and 2-oz (56-g) copper conductor. Construction consists of socket and barrier terminal blocks wave-soldered on an epoxy/glass PC board. RDI/Reed Devices Inc, 21W183 Hill Ave, Glen Ellyn, IL 60137. Circle 258 on Inquiry Card

TRIPLE-OUTPUT, OPEN BOARD POWER SUPPLIES



From 105- to 125-Vac input, model A12T300 offers ±12 Vdc at 300 mA, and 5 Vdc at 2.0 A. Model A15T300 offers ±15 Vdc at 300 mA, and 5 Vdc at 2.0 A. Features common to both include IC regulation of 0.05% line, 0.1% load (no load to full load); low output ripple of <1 mV rms, and 40-h burn-in. Op temp is -25 to 71°C with current limited 150% typ. Options come in ac input voltages. Wall Industries, Inc, 175 Middlesex Tpk, Bedford, MA 01730. Circle 259 on Inquiry Card

PACE-ICOM FLOPPY DISC INTERFACE

Featuring a single PC card which connects to PACE application system bus on one edge and accepts ICOM FD360 controller on the other, interface uses 16-bit commands and data transfer. System can support from one to four drives. Typ IBM format diskette can be read and rewritten in 7.5 s. DOS II monitor listings are included. Optional p/ROM bootstrap plus diskette with DOS II monitor is available. **Abler Data Services, Inc,** 740 Garvens Ave, Brookfield, WI 53005.

Circle 260 on Inquiry Card

MODCOMP.* HARDWARE DEVELOPMENT CAREER OPPORTUNITIES

We are seeking experienced professionals to join us and be a part of our rapid expansion in the booming mini-computer industry. There's never been a better time to consider the outstanding career opportunities with MODCOMP and the good life in sunny Ft. Lauderdale, Florida.

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We are seeking an aggressive thinker to lead the entire computer design activity in an environment providing rapid advancement. Immediate responsibilities include, system conceptual design of all new processors and memory systems, technical management and guidance of a team of senior and junior computer designers and significant contribution to definition and development of a new distributed intelligence network system

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Mr. Robert M. Coyner MODULAR COMPUTER SYSTEMS, INC.

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MODCOMP

HIGH CONTRAST CRT



For high contrast under amb lighting conditions, DC3263 is supplied with medium-long persistence, antiflicker P39 phosphor, and spectrally-matched contrast filter/implosion panel. Spectral emission is between 500 and 550 nm; display trace width is 0.015" (0.0381 cm). For g-p use, metal-cone CRT is available with P31 medium-short persistence phosphor; for radar displays, tube has P33 or multipersistence phosphor. Focus is high voltage electrostatic; deflection is magnetic with a 53-deg angle. **DuMont Electronics Corp**, 750 Bloomfield Ave, Clifton, NJ 07015. Circle 261 on Inquiry Card

10-COLUMN THERMAL PRINTHEAD



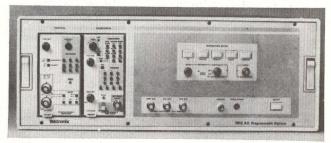
A dot matrix printhead designed for medium speed alphanumeric strip and page printing applications, the DM1050 permits nonimpact printing with the only moving part being the advance mechanism. Character line speeds through 7 lines/s are possible, printing a full 5 x 7 matrix char on std 90°C heat-sensitive paper. Legible high density printout is provided by closely spaced, thermally

coupled dot elements. Printheads are furnished with a soldered ribbon cable and mounted on a std heat sink designed for ganged operation to extend the number of columns. A negligible element TCR eliminates inrush current and the need to overdesign power supply and driver circuitry. MTBF is a min of 10M char-lines at max rated operation. Gulton Industries, Inc, Hybrid Microcircuit Dept, 212 Durham Ave, Metuchen, NJ 08840. Circle 262 on Inquiry Card

SIL SOLID-STATE RELAYS

Optically isolated solid-state units combining thick-film hybrid techniques with tested discrete components, series 7580 general-purpose control relays are rated at 2 A for use as I/O devices between logic level circuits and ac line power. The units occupy <0.5 in³ (8.2 cm³) and take up only 0.5 in² (3.22 cm²) board space. The four pins are spaced to fit existing DIL sockets or can be used on PC board with 0.5" (1.3 cm) centers. Features include zero voltage turn-on, zero current turn-off; 1500-V rms isolation; and polarity protected input. Dimensions are 1.6 x 0.75 x 0.35" (4.1 x 1.9 x 0.89 cm). Right-angle mounting is optional. Hamlin, Inc, Lake & Grove Sts, Lake Mills, WI 53551. Circle 263 on Inquiry Card

PROGRAMMABLE HIGH SPEED WAVEFORM DIGITIZER



Featuring fully programmable operation and compatibility with the IEEE-488 bus, the 7912AD captures transients to 1 GHz (fully programmable to 200 MHz) and performs automatic waveform digitizing. Operation is similar to that of an oscilloscope except that acquired waveforms are output as digital information for waveform processing rather than being presented as CRT displays. A built-in microprocessor enables scale factors and most other controls to be set from a remote terminal or software program. The unit captures single-shot transients up to 500 MHz in conventional operating mode and up to 1 GHz using direct access to CRT deflection plates. Equivalent writing rate is 8000 div/µs. Acquired signals are digitized using a precise raster scanning approach. Tektronix, Inc, PO Box 500, Beaverton, OR 97077. Circle 264 on Inquiry Card



CIRCLE 102 ON INQUIRY CARD



PARTIALLY UNINTERRUPTIBLE **SWITCHING SUPPLY**

With partial UPS capabilities, model 692 allows a system to stay on at reduced capacity until ac returns. Ac input is fed into a switcher inverter which provides 5 V at 100 A and 60 V at 5 A; 60-V output is then fed into input of dc-dc converter which gives 5-V, and 12 to 15-Vdc outputs. Dc-dc converter input is diode coupled to 48-Vdc battery source. Upon removal of the ac input, the 60-Vdc output drops, and battery



supplies input for dc-dc converter (outputs 2 and 3). Reduction in UPS section by 25% to outputs 2 and 3 provides 268 W or 48 Vdc at 6 A. Trio Labs, Inc. 80 Dupont St, Plainview, NY 11803.

Circle 265 on Inquiry Card

INDUSTRIAL DATA **COLLECTION TERMINALS**

One of two basic models in the 1040 line, the 1040-1 MITE (microprocessor industrial terminal) includes microprocessor; 16-char alphanumeric, interactive, self-scan display; and 2-wire party line or RS-232 interface with such options as badge, 22/80-col card, and batch card readers, and terminal printer which prints 2200 char/s. The 1040-2 MATE (microprocessor attendance terminal) reads Hollerith or special-purpose badges and includes clock time readout as well as up to 10 function switches. Essex Engineering Co, Essex, CT 06426.

Circle 266 on Inquiry Card

PRINTERS

heavy-duty 132 Columns 250-720 LPM **Chain Printer** Excellent Quality and Price



If you are an OEM in the computer industry, you know the crucial importance of gaining a competitive edge. We know it, too.

CITIZEN is the largest independent line printer manufacturer in Japan. We are new in the U.S. market. A very tough market. And we are growing fast because we offer our clients a very advantageous price/performance mix. The competitive edge.

The Citizen Series 8000 Line Printers are available in two basic models, with the following minimum speeds:

Model 8201 Model 8601 298 LPM — 48 characters — 720 LPM 250 LPM — 64 characters — 600 LPM 188 LPM - 96 characters - 444 LPM

Full details on the competitive edge offered by the Citizen Series 8000 printers are yours for the asking.

Mike M. Fujiwara Marketing Manager, Line Printers C. ITOH ELECTRONICS, INC. 5301 Beethoven Street Los Angeles, California 90066 Telephone: 213/390-7778



C C. ITOH ELECTRONICS, INC.

CITIZEN SERIES 8000

Manufactured by CITIZEN WATCH CO. Tokyo, Japan

Interior view of printer mechanism Font train

CPU BOARD

For use as a standalone computer or as the CPU in a larger system, model 500 accepts 8k of ROM, 4k of RAM, 750 bytes of p/ROM, an ACIA-based serial port, a 6502 processor, and full buffering for expansion. Completely assembled with 8k BASIC in ROM, the board requires 5 V at 2 A, -9 V at 500 mA, an external reset switch, and an ASCII serial terminal for operation. Serial interface is jumper selectable for RS-232-C or 20-mA current loop at 110, 300, 1200, 2400, or 4800 baud. Ohio Scientific, Hiram, OH 44234. Circle 267 on Inquiry Card

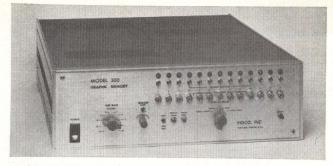
MASS TERMINATED 50-CONDUCTOR CABLES

Insulation displacement enables the Vitel-F connector to be mass terminated in the field with up to 50 conductors, and reterminated if necessary to change the conductor pattern within the connector. A stable and minimal contact resistance is achieved by pressing conductors into place on a carrier strip. The resultant mechanical coupling consists of four contact-to-conductor junctions with an apparent junction area of up to 1000 circular mils/coupling. Viking Industries, Inc, 21001 Nordhoff St, Chatsworth, CA 91311. Circle 268 on Inquiry Card

12-BIT S-D CONVERTER

SDC-632 series conversion rates are 0 to ±300 r/min, error free. Broadband inputs between 360 and 1k Hz are accepted and accuracy is ±8.5 min of arc. Using a ratiometric technique, device is insensitive to voltage/frequency variations. Internal CMOS logic reduces power consumption to <225 mW. In addition to logic voltage supply, only 15 Vdc is required. The 15-V nominal supply ranges from 11 to 17 V. Logic supply range is 4.5 Vdc to positive supply voltage to accommodate TTL, DTL, or CMOS. ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716. Circle 269 on Inquiry Card

SOLID-STATE GRAPHIC MEMORY



Model 300 YT accepts analog signals, converts them to digital form, and stores them in MOS memory where they are available for continuous television display or video recording. The unit accepts and makes available for display up to 13 inputs simultaneously. Signals are plotted against an internal time base. Front panel switches permit easy selection of one or any combination of inputs for immediate display. Features include store, auto-erase, single-sweep, and wipe display modes. A visible marker shows the location of the sweep as the display is updated. Trigger source selection includes channel 1, external, or free-running. Options are available to meet specialized requirements. **Vidco Inc**, PO Box 25452, Portland, OR 97225.

DATA ACQUISITION MODULE

1

1

7

Combining several high speed data acquisition modules into a 16-channel A-D subsystem, the DAS-250 eliminates the difficulties and special techniques required to assemble a 250-kHz data acquisition system. The unit consists of two 4.25 x 5.00" (10.79 x 12.7-cm) PC boards joined by 1" (2.5-cm) standoffs. As an analog front end for mini- and microcomputers, the unit will store an A-D sample and its corresponding 4-bit channel address in its double-buffered output. The computer can take this sample while the next A-D conversion is in progress. It operates in sequential or random channel addressing modes. Overall accuracy is ±0.025%, ±1 LSB. Resolution is 12 binary bits. Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021.

INDUSTRIAL OPTICAL SWITCH



The 113-X is a completely self-contained device that requires no external power source, and will switch up to 6 A of ac load. Electronics are rugged but simple; when a mechanical interrupter is removed, a lensed LED actuates a similarly lensed phototransistor across an air gap. The phototransistor activates a solid-

state relay rated at 1- or 6-A ac current. Model 113-1 is a 6-A version in a rugged aluminum case; the -2 is a 1-A version in a heavy duty molded plastic package. Features include rapid response, long life (expected 50M operations), bounce-free switching, and shock and chemical resistant housing. The solid-state unit is completely isolated from switching voltage. **HEI, Inc,** Jonathan Industrial Ctr, Chaska, MN 55318.

Circle 272 on Inquiry Card



CIRCLE 105 ON INQUIRY CARD



LITERATURE

LSI Design

Design catalog covering line of data conversion, timing, and linear LSI products provides PCB layouts and construction tips, and describes IC functions and operating characteristics. Siliconix, Inc, Santa Clara, Calif.

Circle 300 on Inquiry Card

Environment-Sealed Switches

Hll series featuring the building block approach to custom switch design is depicted in bulletin containing electrical/mechanical specs, housing dimensions, and options. Control-Switch, a Cutler-Hammer Co, Folcroft, Pa.

Circle 301 on Inquiry Card

Direct Connect Modems

Brochure describes the 317 series of 300-bit/s modems, and lists configurations involving the multiple data sets VA1616 and -1601. Vadic, Mountain View, Calif. Circle 302 on Inquiry Card

High Voltage Testing

Basic Facts About High Voltage Testing, a 20-page manual with charts and photos, includes a section on safety considerations to aid both the novice and expert. Slaughter Co, Ardmore, Okla.
Circle 303 on Inquiry Card

Extruded Heat Sinks

Technical bulletin lists dimensions, weights, thermal resistances, and heat-dissipating surfaces of extruded heat sinks for medium and high power semiconductors. International Electronic Research Corp, Burbank, Calif.

Circle 304 on Inquiry Card

Modular Power Supplies

Handbook outlines current practices and terminology, presents specs in tabular form, and gives case/pin configurations for line-operated power supplies and dc-dc converter modules. Datel Systems, Inc, Canton, Mass.

Circle 305 on Inquiry Card

Terminals and Splices

Catalog covering insulated and noninsulated construction for terminals, splices, and disconnects has drawings, charts, graphs, and specs for high temp applications. ITT Cannon Electric, ETC Terminal Products Unit, Solon, Ohio. Circle 306 on Inquiry Card

Electronic Connectors

Brochure with capabilities and design guide includes specs, mechanical drawings, and features for PC card-edge connectors, DIP sockets, and backpanels.

Dynatech Corp, Santa Ana, Calif.

Circle 307 on Inquiry Card

Power Supplies

Application and selection guide presents test procedures, electrical/mechanical specs, dimensional drawings, and options for line-operated and dc-dc converter power supplies. Semiconductor Circuits, Inc, Haverhill, Mass.

Circle 308 on Inquiry Card

IC Interconnection

Data sheet on IC interconnection packaging devices and accessories, such as DIP sockets, strip receptacles, and substrate sockets, covers physical and electrical characteristics, features, and schematics. AMP, Inc, Harrisburg, Pa.

Circle 309 on Inquiry Card

A-D/D-A Conversion Modules

Brochure with tables and curve plots supplies features, specs, and operating parameters for line of A-D/D-A converters, multiplexers, sample/holds, and power supplies. Analogic, Wakefield, Mass. Circle 310 on Inquiry Card

Fiber Optic Design

Historical perspectives, economic and design advantages, applications, and details of the design system make up brochure on analog/digital transmission with fiber optics. Valtec Corp, Fiberoptics Div, West Boylston, Mass.

Circle 311 on Inquiry Card

V-F-V Converters

Illustrated with block diagrams, applications bulletin offers solutions to a variety of problems related to frequency-to-voltage and voltage-to-frequency conversion. **Teledyne Philbrick**, Dedham, Mass. Circle 312 on Inquiry Card

Desktop Computer

The 9831A BASIC-language desktop computer is described in illustrated brochure which summarizes related features, applications, software, and peripherals. Hewlett-Packard Co, Palo Alto, Calif.

Circle 313 on Inquiry Card

TV CRT Graphics Controller

Data bulletin, spec sheet, and application note with block diagrams detail applications and utilization of 256 x 256 graphics display controllers for interfacing a microprocessor and TV monitor. Matrox Electronic Systems, Montreal, Canada. Circle 314 on Inquiry Card

Logic Interface

Handbook with wiring diagrams reviews control systems languages and compares programmable controllers to hardwired systems to explain interfacing solid-state position sensors and manual switches with industrial control systems. Micro Switch, div of Honeywell, Freeport, Ill. Circle 315 on Inquiry Card

Real-Time Systems

Describing hardware and software components of systems based on the PDP-11 family, brochure covers operating systems, high level languages, application-oriented software, and configurations. Digital Equipment Corp, Communication Services, Northboro, Mass.

Circle 316 on Inquiry Card

Array Processors

AP-1208 floating point array processor is the subject of literature package consisting of application notes and booklet discussing state-of-the-art development and architecture. Floating Point Systems, Inc, Portland, Ore. Circle 317 on Inquiry Card

Instrumentation Controller

Model 3530 designed for IEEE 488 bus compatibility applications is outlined in brochure presenting features, specs, system configuration, and related software. Systron Donner Corp, Data Products Div, Concord, Calif.

Circle 318 on Inquiry Card

Stroboscopes

To aid in the design of disc and tape mechanisms, Handbook of Stroboscopy explores the slow and stopped motion illusion of motion analysis, high speed photography, and applications. GenRad, Inc, Concord, Mass.

Circle 319 on Inquiry Card

Memory and Microcomputer Systems Design

Three reports highligh major trends in microcomputer system design—the use of high density dynamic RAMS (APR-1); the MCS-48 family of single-chip microcomputers (AP-24); and the SBC 80/10, System 80/10 microcomputer-based open computers (AP-26). Send \$1 for each to: Literature Dept, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051.

GUIDE TO PRODUCT INFORMATION

PAGE	PAGE	PAG
MATERIALS	Power Supply Tester	Micronycon
PLASTICS AND PLASTIC FORMS	Autotest172	Advanced Micro Devices 20 2
Polyurethane Structural Foam Mobay Chemical69	RELAYS	Motorola Semiconductor Products58, 5
69	Solid-State Relays Hamlin191	nockwell International/Microelectronic
HARDWARE	reledyne Helays190	Devices112, 11
CONNECTORS AND INTERCONNECTION	Miniature PC Relays	Data Acquisition System Burr-Brown13
SYSTEMS	Arrow-M	D-A Converter
Connectors AMP44, 45	Ground Fault Relay System	Analog Devices70, 7
Amprience North American/Bunker	Gould/Switchgear189	Companding DAC
I/O Connectors	SENSORS; TRANSDUCERS	Precision Monolithics
Positronic Industries182	Vane Position Sensors Micro Switch/Honeywell184	LINEAR INTEGRATED CIRCUITS BIFET Op Amps
Edge Connectors	SWITCHES	Precision Monolithics188
SMK Electronics188	DIP Switches	Phase Locked Loop
Texas Instruments/Metallurgical Materials184	Grayhill151	Signetics166
Flat Cable Connector System	Miniature Toggle Switches	MEMORY/STORAGE EQUIPMENT
3M104	Raytheon/Distributor Products Operation180	FLEXIBLE DISC UNITS
50-Conductor Cable Connector System Viking Industries192	Programmable Solid-State Switches	Flexible Disc Drives
Ribbon Cable Wiring Harness	Computer Conversions183	General Systems Int'l.
AMP/Special Industries186	Pushbutton Switch Modules Centralab Electronics/Globe-Union 93	Micro Peripherals 178 Shugart Associates 146, 147
INDICATORS; READOUTS;	Touch Switch Panel	Flexible Disc Systems
DIGITAL DISPLAYS; LAMPS Liquid Crystal Display	Centralab Electronics/Globe-Union 93	Charles River Data Systems
Epson America178	THERMAL COMPONENTS	Wangco/Perkin-Elmer Data Systems130, 131
Alphanumeric Display Subsystems	Thermostats	Flexible Disc System Kits
Industrial Electronic Engineers184	Elmwood Sensors165	Southwest Technical Products176
MOUNTING HARDWARE	CIRCUITS	Flexible Disc Controller
PC Card Locking Device Unitrack/Calabro Plastics176		Intel128 Flexible Disc Interface
SHIELDING	CIRCUIT CARDS AND MODULES Core Memory Boards	Abler Data Services190
Shielding Components	Dataram	MAGNETIC CORE MEMORIES
Instrument Specialties187	Fabri-Tek177	Core Memory Systems
SOCKETS	CCD Memory Board Alpha Data126	Dataram
Sockets	ROM Board	MAGNETIC DISC AND DRUM UNITS
Robinson Nugent62, 63 Relay Socket Assemblies	Infotek Systems196	(See also Flexible Disc Units)
RDI/Reed Devices190	Semiconductor Memory Boards Fabri-Tek186	Cartridge Disc Drives
	Intel Memory Systems 143	Diablo Systems/XeroxCover IV
COMPONENTS AND ASSEMBLIES	Monolithic Systems 122 123	Disc System Singer/Librascope185
DELAY LINES	Motorola Integrated Circuits	Disc Mass Memory
Low Cost Delay Line Pulse Engineering184	Microcomputer Systems176	Alpha Data186
ELECTRON TUBES; CRTS	Flexible Disc Interface	Disc Controllers Dataflux183
High Contrast CRT	Abler Data Services190 Interface Boards	Microcomputer Systems176
DuMont Electronics190	MDB Systems118	MAGNETIC TAPE UNITS
MOTORS; ROTATIVE COMPONENTS	I/O Boards	Tape System
Motors	Adac	Datum
Hitachi America	DIGITAL AND INTERFACE INTEGRATED	Micro Communications189
Pittman/Penn Engineering &	CIRCUITS	Tape Drives
Manufacturing 22	Field Programmable Logic Array	Pertec Computer
North American Philips Controls189	Texas Instruments/Components 55 Correlator IC	Digi-Data
	TRW/LSI Products137	Kennedy 1
PHOTODEVICES; PHOTODEVICE ASSEMBLIES Industrial Optical Switch	12-Bit Multiplier	Cartridge Tape Drives 3M/Mincom160, 161
HEI193	TRW162 OR/NOR IC	MFE
POWER SOURCES, REGULATORS,	Plessey Semiconductors166	Cassette Recorder
AND PROTECTORS	Schottky Cell Array IC	Braemar Computer Devices191 Magnetic Tape Controller
Power Equipment Pacific Electronic Enterprises200	Hughes Aircraft/Microelectronic Products166	Aviv188
Power Supplies	CCD Memory	Magnetic Tape
Acme Electric183	Fairchild Semiconductor19-21	Pericomp193
CPS	Static RAMs Creative Micro Systems144	MEMORY/STORAGE TEST EQUIPMENT Tape and Disc Drive Exercisers
Digital Power180	Mostek75	Wilson Laboratories
Gould/Power Supply134, 135 Wall Industries190	VMOS RAM	ROM/RAM PROGRAMMERS AND SIMULATORS
Microprocessor Power Supplies	American Microsystems16, 17 RAM-I/O Device	p/ROM Programmer/Emulator
Hewlett-Packard157	National Semiconductor132	Sunrise Electronics138
Switching Power Supply Kepco190	8k and 16k EPROMs	SEMICONDUCTOR MEMORIES
Semi-Uninterruptible Switching Power Supply	Intel Memory Systems36, 37	CCD Memory
Trio Labs192	Fairchild Semiconductor133	Fairchild Semiconductor19-21 Static RAMs
Switching Regulators Sola Electric188	Motorola Semiconductor156	Creative Micro Systems144
	Signetics136	Mostek75

GUIDE TO PRODUCT INFORMATION

	PAGE
DISPLAY EQUIPMENT	
(See also Data Terminals and Graphic Equipment)	
Frameless CRT Display Ball/Electronic Display	176
RAM Video Interface Computer Technology	144
GRAPHIC EQUIPMENT	
Graphics System Megatek	178
Graphic Display System Ramtek	72, 73
Graphic Display Terminal Ramtek	47
Modular Graphics Display Terminal Tektronix/Info. Display Group	
Data Tablets and Digitizers Summagraphics	
Sonic Digitizer Science Accessories	
Video Digitizer/Display DeAnza Systems	183
INTERFACE EQUIPMENT; CONTROLLE	RS
Interface Boards MDB Systems	118
Flexible Disc Interface Abler Data Services	190
Flexible Disc Controller Intel	128
Disc Drive Controllers Dataflux Microcomputer Systems KEYBOARD EQUIPMENT	183 176
Keyboards Micro Switch/Honeywell OTHER INPUT/OUTPUT EQUIPMENT	120g
PDP-11 Systems Bus Repeater Datafusion	186

Hewlett- Packard Packard
983 You can now dimension, sort You can now dimension, sort and search any array that and search any array memory.
Will fit in your The Will Infotek's Fast Basic III With Infotek's Fast Basic III ROM the 256 row-column limit ROM the 25

CIRCLE 114 ON INQUIRY CARD

PLOTTING EQUIPMENT
Digital Plotters Axiom145
Zeta Research182
PRINTER/PLOTTERS
Line Printer/Plotter Printronix163
PRINTING EQUIPMENT Printers
C. Itoh Electronics
OEM Printer Teletype171
Line Printers
Epson America
Serial Printer Florida Data
Impact Printer Motorola Microsystems
Matrix Drintore
Control Data
Digital Printers C. Itoh Electronics199
Alphanumeric Printers Datel Systems
Sheldon-Sodeco Printer
Dataproducts
Gulton Industries/Hybrid Microcircuit191 PUNCH CARD EQUIPMENT
Hostile Environment Card Reader AMP/Capitron176
PUNCHED TAPE EQUIPMENT
Punched Tape Reader EECO14
Tape Reader/Punch Sweda International/OEM Products184
Tape Perforators Ex-Cell-O/Remex187
SOURCE DATA COLLECTION EQUIPMENT
SOURCE DATA COLLECTION EQUIPMENT Data Collection Terminals
Data Collection Terminals
Data Collection Terminals
Data Collection Terminals Epic Data
Data Collection Terminals
Data Collection Terminals
Data Collection Terminals Epic Data
Data Collection Terminals Epic Data
Data Collection Terminals Epic Data Essex Engineering
Data Collection Terminals Epic Data
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data Essex Engineering
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data 174 Essex Engineering 192
Data Collection Terminals Epic Data

P

Miniature Panel Counter

PAGE
LSI-11 Time/Date Units Digital Pathways186
DIGITAL EQUIPMENT TESTERS
Digital Test Equipment Tektronix66, 67
Logic Probes Continental Specialties169
Kurz-Kasch/Electronics191
Logic Analyzers Biomation172
Hewlett-PackardCover II Signature Analyzer
Hewlett-Packard117
Digital/Analog Automatic Test System GenRad185
Memory Test Systems Teradyne94
Tape and Disc Drive Exercisers Wilson Laboratories
Microprocessor Test System
Adar Associates
RFL Industries184
DIGITIZERS Programmable Waveform Digitizer
Tektronix191
Video Digitizer/Display DeAnza Systems183
Solid-State Graphic Memory Vidco193
OTHER TEST AND MEASUREMENT EQUIPMENT
Accelerometer Impact-O-Graph187
Power Supply Tester Autotest172
OTHER PRODUCTS; SERVICES
EDUCATION
Seminars Integrated Computer Systems140, 141
EMPLOYMENT OPPORTUNITIES
Employment Opportunities Modular Computer Systems190
NCR Terminal Systems/ Cambridge
EQUIPMENT BUYING, SELLING, AND LEASING
Computer Equipment Rentals Leasametric/Metric Resources
Microcomputer Equipment Rentals
Rental Electronics 61 Computer Equipment Sales
Newman Computer Exchange193 EXHIBITIONS
Conference/Exhibition
Industrial & Scientific Conference Management197
Computer Conference/Exhibition Mini/Micro Computer Conference120h
Computer Conferences
Invitational Computer Conference 78 INSTITUTIONAL
Computers and Peripherals Perkin-Elmer Data Systems
MARKET REPORTS
Custom Market Surveys Computer Design Market Research188
OTHER NON-DIGITAL PRODUCTS
Security Systems Motorola Government Electronics154
PLANT LOCATION
Plant Location Puerto Rico Economic
Development Administration 92 SOFTWARE
Software
Forth
Dynalogic
muPro

Michael Shrayer176

Software Cross-Assemblers

Call-Data Systems

.....188

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ADVERTISERS' INDEX

Advanced Micro Devices	28.	29	Lear-Siegler, Inc.	139, 166, 167
American Microsystems Inc.	10,	17	1 and a late	
Alpha Data Inc		120	Div. of Metric Resources Corp.	13
AMP, Inc.	44,	45		
Amphonal North American Div.				104
Bunker Pamo Corp	Cover	71	3M Co. Mincom Div.	160, 161
Analog Devices, Inc.	/0,	145	MDB Systems, Inc.	118
Axiom Corp.		נדו	Megatek Corp.	178
			MEE Corp	159
Braemar Computer Devices, Inc.		191	Micro Communications Corp.	189
Burr-Brown Research Corp.		127	Minne Switch	
			a div. of Honeywell	120g
CallData Systems, Inc.		119	Mini/Micro Computer Conference and Exhibition	120n
C I I I Flantanias Div			Mobay Chemical Corp. Modular Computer Systems, Inc.	190
Globe-Union, Inc.		183	Monolithic Systems Corp.	122, 123
Charles River Data Systems, Inc. Computer Design Publishing Corp.		188	Mostek	75, 77
Computer Automation, Inc.	52	53	Materials Inc	
Computer Products, Inc.		7	Gavernment Flectronics Div	154
Control Data Corp.		12/	Motorola Semiconductor Products, Inc.	58, 59
Conrac Corp		181		
Continental Specialties Corp.		169		152 152
Cutler-Hammer, Inc.		19	National Semiconductor Corp.	152, 153
			NCR Corp., Terminal Systems Div.	199
Data General Corp.	35,	173	NEC Microcomputers Inc	00
Dataram Corp		171	Newman Computer Exchange	193
Dataproducts	80	, 81	Mandon Div	
Datum, Inc.		26	United Tachnologies Corn	43
Diablo Systems, Inc.	20 Cove	r IV	North American Philips Controls Corp.	189
a Xerox Co. Digi-Data Corp.	37, 0076	31		
Digital Equipment Corp.	40	. 41		200
Digital Equipment Corp.			Pacific Electronic Enterprises, Inc.	200
		1.4	Pericomp	23
EECO		14	Perkin-Elmer Data Systems Pertec Computer Corp.	56. 57
Elmwood Sensors, Inc.		174	Pittman Corp.	22
Epic Data Corp. Epicom, Inc.		179	Printronix Inc	103
Epson America, Inc.		76	Puerto Rico Economic Development Administration	92
Epson America, me				
		. 177		47 70 73
Fabri-Tek, Inc. Fairchild Semiconductor Corp.	19-21	133	Ramtek Corp.	47, 72, 73
Florida Data Corp.	/ - 2. 1	155	Rental Electronics, Inc.	42 63
Forth, Inc.		175	Robinson Nugent, Inc.	
Futuredata Computer Corp.	48	3, 49	Rockwell International, Microelectronic Devices	112, 113
			Rolm Corp.	51
General Systems International		1200	Kolili Gorp.	
		1200		
Gould, Inc., Power Supply Div	134	135	Shugart Associates	146, 147
Grayhill, Inc.		151	C: C-	
			Liberrana Div	185
	. II 117	157	Summagraphics Corp.	7
Hewlett-Packard CompanyCove	21 11, 117	30	Sweda International, Inc., OEM Products Div.	184
Honeywell Information Systems		. 82	OEM Products DIV	10, 11
Houston Instrument			Systems Engineering Laboratories	
Div. of Bausch & Lomb		. 180		
			Tally Corp.	2
Integrated Computer Systems	140	141	Toktroniy Inc	8, 9, 00, 07
Impact-O-Graph Corp.		187	Information Display Group	
Industrial & Scientific Conference Management, Inc.		. 197	Talatuna Corn	1/1
Infotek Systems		. 196	Teradyne Inc.	75
Instrument Specialties Co., Inc.		. 187	TEXAS INSTRUMENTS INCORPORATED, Components Div.	55
Intel Memory Systems	36, 37	, 143	TRW LSI Products	
Intelligent Systems Corp.	1	4, 10	TRVV ESI Floudels	
Interdata, Inc., a unit of Perkin-Elmer Data Systems		. 5		
Interface Mechanisms				
Interstate Electronics		. 186	Wangco, Inc.,	
		186 120c	- wit of Porkin Elmer Data Systems	130, 13
Invitational Computer Conference		186 120c 78	a unit of Perkin-Elmer Data Systems	130, 13
Invitational Computer Conference C. Itoh Electronics, Inc.		186 120c 78	a unit of Perkin-Elmer Data Systems	130, 13
Invitational Computer Conference	192	186 120c 78	a unit of Perkin-Elmer Data Systems	/'
Invitational Computer Conference C. Itoh Electronics, Inc.	192	186 120c 78 2, 199	a unit of Perkin-Elmer Data Systems Wilson Laboratories, Inc. Zeta Research Corp.	
Invitational Computer Conference	192	186 120c 78 2, 199	a unit of Perkin-Elmer Data Systems Wilson Laboratories, Inc. Zeta Research Corp.	

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